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?s pn=cn 1069828
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2/5/1   (Item 1 from file: 345)

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Basic Patent (No,Kind,Date): CN 1124620 A 19960619   <No. of Patents: 002>

PATENT FAMILY:
CHINA (CN)
   Patent (No,Kind,Date): CN 1124620 A   19960619
      CONTRACEPTIVE (English)
      Patent Assignee: YU QIWAN (CN)
      Author (Inventor): QIWAN YU (CN)
      Priority (No,Kind,Date): CN 94119584 A   19941215
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      IPC: * A61K-031/155
      CA Abstract No: ; 128(26)326491C
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      Language of Document: Chinese
   Patent (No,Kind,Date): CN 1069828 B   20010822
      CONTRACEPTIVE (English)
      Patent Assignee: YU QIWAN (CN)
      Author (Inventor): YU QIWAN (CN)
      Priority (No,Kind,Date): CN 94119584 A   19941215
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      CA Abstract No: * 128(26)326491C
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009256263   **Image available**
WPI Acc No: 1992-383676/199247
XRPX Acc No: N92-292556
  **Multiple electrode field electron emission device for use e.g. as linear
  amplifier - has cathode emitter tips with reduced radius of curvature and
  low threshold voltage with self-aligned gate electrode**
Patent Assignee: SEIKO EPSON CORP (SHIH); SEIKO EPSON CO LTD (SHIH)
Inventor: KOMATSU H
Number of Countries: 012 Number of Patents: 010
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 513777	A2	19921119	EP 92108110	A	19920513	199247	B
JP 5182582	A	19930723	JP 9280380	A	19920302	199334	
EP 513777	A3	19931020	EP 92108110	A	19920513	199510	
US 5386172	A	19950131	US 92882436	A	19920513	199511	
TW 255051	A	19950821	TW 92102596	A	19920406	199543	
CN 1069828	A	19930310	CN 92104552	A	19920512	199705	
JP 3235172	B2	20011204	JP 9280380	A	19920302	200203	
JP 2001351507	A	20011221	JP 9280380	A	19920302	200206	
			JP 2001109747	A	19920302		
JP 2002163998	A	20020607	JP 9280380	A	19920302	200241	
			JP 2001237471	A	19920302		
JP 2002134000	A	20020510	JP 2001237471	A	19920302	200246	
			JP 2001268212	A	19920302		

Priority Applications (No Type Date): JP 9280380 A 19920302; JP 91107505 A
   19910513; JP 91164636 A 19910704; JP 91186203 A 19910725; JP 91222088 A
   19910807; JP 91309757 A 19911029
Cited Patents: No-SR.Pub; 1.Jnl.Ref; EP 172089; EP 316214; EP 376825; EP

400406; EP 406886; EP 444670; JP 53121454; US 5012153; WO 9102371
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 513777	A2	E	43	H01J-001/30	
Designated States (Regional): CH DE FR GB IT LI NL SE					
JP 5182582	A			H01J-001/30	
EP 513777	A3			H01J-001/30	
US 5386172	A		47	H01J-001/02	
TW 255051	A			H01J-021/14	
CN 1069828	A			H01J-019/42	
JP 3235172	B2		22	H01J-021/06	Previous Publ. patent JP 5182582
JP 2001351507	A		22	H01J-001/304	Div ex application JP 9280380
JP 2002163998	A		23	H01J-029/04	Div ex application JP 9280380
JP 2002134000	A		21	H01J-001/304	Div ex application JP 2001237471

Abstract (Basic): EP 513777 A
    The device has a cathode (3) for emitting electrons using the field effect from multiple emission projections (4). A gate electrode(s) establishes an electric field between the cathode and the gate electrode. An anode (7) collects the emitted electrons. A control electrode (6) is placed between the cathode and the anode for controlling the emitted electrons.
    Pref. a screen electrode electrostatically screens the control electrode and the anode. A suppressor electrode is palced between the scree electrode and the anode for controlling secondary electrons emitted from the anode.
    USE/ADVANTAGE - Cathode emission projections with curvature radius of 40nm. Large gate input resistance. Linear input output transfer characteristics with large anode resistance. Equivalent current, voltage and power handling capability to conventional vacuum tubes. Small size. Flexible circuit configurations, with frequency power efficiency or voltage characteristics tailored to specific application. High speed operation possible.
    Dwg.1/33

Title Terms: MULTIPLE; ELECTRODE; FIELD; ELECTRON; EMIT; DEVICE; LINEAR; AMPLIFY; CATHODE; EMITTER; TIP; REDUCE; RADIUS; CURVE; LOW; THRESHOLD; VOLTAGE; SELF; ALIGN; GATE; ELECTRODE
Derwent Class: U11; U12; V05
International Patent Class (Main): H01J-001/02; H01J-001/30; H01J-001/304; H01J-019/42; H01J-021/06; H01J-021/14; H01J-029/04
International Patent Class (Additional): H01J-001/16; H01J-001/46; H01J-009/00; H01J-009/02; H01J-019/24; H01J-021/00; H01J-021/10; H01L-021/00; H03F-003/02
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[54]发明名称　多极场致电子发射器件及其制造方法

[57]摘要

　　一种多极场致电子发射器件，它形成于一绝缘层上，而该绝缘层形成于一绝缘平基片表面上，该器件至少包括：一个阴极，它具有多个伸出所述绝缘层的发射尖端；一个阳极，它形成于所述绝缘平基片的表面上，并收集从发射尖端发射的电子；一个控制电极，它形成于所述阴极与阳极之间。该器件是采用过蚀刻和定向粒子淀积方法制造的。

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(BJ)第 1456 号
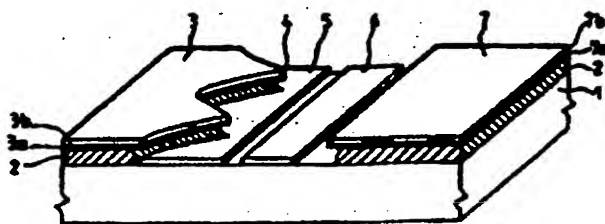
1. 一种多极场致电子发射器件，其特征在于，至少包括：一个借助场效应发射电子的阴极，一个把电场加到所述阴极的栅极，一个收集发射电子的阳极，和一个控制电极，该控制电极位于所述的阴极和阳极之间，并控制所述的发射电子。

2. 根据权利要求1所述的多极场致电子发射器件，其中，一个静电屏蔽控制电极和阳极的屏蔽电极位于控制电极和阳极之间。

3. 根据权利要求1所述的多极场致电子发射器件，其中，一个静电屏蔽控制电极和阳极的屏蔽电极位于控制电极和阳极之间，一个控制阳极的二次电子的抑制电极位于所述屏蔽电极和阳极之间。

4. 一种多极场致电子发射器件，其特征在于，至少包括：一个在绝缘平基片表面上形成的岛状绝缘层；一个备有发射尖端的阴极，此发射尖端位于前述岛状绝缘层的表面上并从该岛状绝缘层伸出；一个栅极，它形成于所述平基片的表面上，并几乎与所述发射尖端的邻近区域正交；一个阳极，它形成在平基片表面上所述阴极的对侧，所述栅极位于此阳极与阴极之间；以及一个控制电极，它形成于所述平基片表面上所述栅极与阳极之间。

5. 根据权利要求4所述的多极场致电子发射器件，其中，一个屏蔽电极形成于平基片的表面上控制电极与阳极之间。

6. 根据权利要求4所述的多极场致电子发射器件，其中，一个屏蔽电极形成于平基片表面上控制电极与阳极之间，一个抑制电极形成于平基片表面上屏蔽电极与阳极之间。

7. 根据权利要求4所述的多极场致电子发射器件，其中，控制电极结构的一部分是位于平基片表面上的近似柱形结构。

8. 根据权利要求5所述的多极场致电子发射器件，其中，控制电极和屏蔽电极结构的一部分是位于平基片表面上的近似柱形结构。

9. 根据权利要求6所述的多极场致电子发射器件，其中，控制电极和屏蔽电极结构的一部分是位于平基片表面上的近似柱形结构。

10. 一种多极场致电子发射器件，其特征在于包括：一个铅锤形阴极，它形成于导电的平基片表面上，并具有一个几乎垂直的铅轴；一个第一绝缘层，它形成于平基片表面上，并且围绕所述阴极的周边是开口的；一个栅极层，它形成于所述第一绝缘层的表面上，并且围绕所述阴极的周边是开口的；一个阳极层，它形成于位于一真空层另一侧的对置的平基片表面上；以及一个控制电极，它形成于所述栅极与阳极之间。

11. 一种用于多极场致电子发射器件的驱动方法，其特征在于，把阴极接地；把正偏置栅极电压加到栅极上；把正偏置阳极电压加到阳极上，该电压通常大于栅极电压；以及把输入信号电压加到控制电极上，以便控制阳极电流。

12. 一种用于多极场致电子发射器件的驱动方法，其特征在于，把栅极接地；把负偏置阴极电压加到阴极上；把正偏置阳极电压加到阳极上；以及把输入信号电压加到控制电极上，以便控制阳极电流。

13. 一种用于多极场致电子发射器件的驱动方法，其特征在于，把栅极接地；通过一个和阴极串联的电阻，把负偏置阴极电压加到阴极上；把正偏置阳极电压加到阳极上；以及把输入信号电压加到控制电极上，以便控制阳极电流。

14. 一种用于多极场致电子发射器件的驱动方法，其特征在于，把栅极接地；把负偏置阴极电压加到阴极上；把正偏置屏极电压加到

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屏蔽电极上；以及把输入信号电压加到控制电极上，以便控制阳极电流。

15. 一种用于多极场致电子发射器件的驱动方法，其特征在于，把阴极和抑制电极接地；把栅极电压加到栅极和屏蔽电极上；把阳极电压加到阳极上；以及把输入信号电压加到控制电极上，以便控制阳极电流。

16. 一种多极场致电子发射器件，它包括：一个在绝缘层上形成的阴极，该绝缘层是在一平基片表面上形成的，该阴极有多个从所述绝缘层伸出的发射尖端；一个在所述平基片表面上形成的阳极，它收集发射的电子；一个在所述阴极和阳极之间形成的栅极，它至少在相应于所述发射尖端的位置的一个区域具有开口；以及一个在所述栅极和所述阳极之间形成的控制电极。

17. 一种多极场致电子发射器件，包括：一个在绝缘层上形成的阴极，该绝缘层是在一平基片表面上形成的，该阴极有多个从所述绝缘层伸出的发射尖端；一个在所述平基片表面上形成的阳极，它收集发射的电子；一个在所述阴极与阳极之间形成的栅极，它至少在相应于所述发射尖端位置的一个区域具有开口；一个在所述栅极和阳极之间形成的控制电极；以及一个在所述控制电极和阳极之间形成的屏蔽电极。

18. 一种多极场致电子发射器件，包括：一个在绝缘层上形成的阴极，该绝缘层是在一平基片表面上形成的，该阴极有多个从所述绝缘层伸出的发射尖端；一个在所述平基片表面上形成的阳极，它收集发射的电子；一个在所述阴极和阳极之间形成的栅极，它至少在相应于所述发射尖端的位置的一个区域具有开口；一个在所述栅极和阳

极之间形成的控制电极；一个在所述控制电极和阳极之间形成的屏蔽电极；以及一个在所述屏蔽电极和阳极之间形成的抑制电极。

19．根据权利要求16、17或18所述的多极场致电子发射器件，其中，开口位于与多个发射尖端的位置相应的全部区域。

20．根据权利要求16、17或18所述的多极场致电子发射器件，其中，第二开口位于控制电极上，并与所述的开口相对应。

21．一种场致电子发射器件的制造方法，其特征在于，该器件包括一个发射尖端，该尖端几乎与平基片表面相平行地伸出，并包括至少一个位于所述平基片表面上的蚀刻掩模层，一个位于所述蚀刻掩模层表面上的阴极层，该制造方法包括：在阴极层表面上淀积和形成一个蚀刻钝化层的工序，处理前述蚀刻掩膜层和形成具有发射尖端的蚀刻掩模的工序，以及在前述蚀刻掩膜的平表面上形成前述的阴极层和形成具有发射尖端的阴极的工序。

22．一种场致电子发射器件的制造方法，其特征在于包括：在平基片表面上制造蚀刻掩模层的工序，在蚀刻掩模层表面上形成阴极层的工序，在所述阴极层表面上形成光致抗蚀剂层的工序，在平面状光致抗蚀剂层中处理所述阴极层的工序，利用过蚀刻方法处理蚀刻掩模层形成蚀刻掩模的工序，按蚀刻掩模的形状处理所述阴极层形成阴极的工序，从阴极较低的周边除去所述的蚀刻掩模形成檐状阴极的工序，利用粒子淀积方法形成栅极层的工序，以及处理所述栅极层形成栅极的工序。

23．一种多极场致电子发射器件，包括：一个在绝缘层上形成的阴极，该绝缘层是在一平基片的表面上形成的，该阴极有多个从所述绝缘层伸出的发射尖端；一个在平基片表面上形成的阳极，它收集

发射的电子，该多极场致电子发射器件有这样一个结构，该结构包括多个柱形栅极，这些栅极在所述阴极和阳极之间形成，其中，所述的发射尖端位于相邻栅极的中间，所述栅极的形状为一个凸台，该凸台与阴极侧面上的所述尖端的位置相对应。

24. 根据权利要求23所述的多极场致电子发射器件，其中，栅极是五角柱形的。

25. 根据权利要求23所述的多极场致电子发射器件，其中，栅极比所述发射尖端做得高。

26. 一种制造权利要求23所述的多极场致电子发射器件的方法，它包括下述工序：在绝缘平基片表面上依次形成一个绝缘层和一个电极层，然后，在置留下栅极的平面图形和涂覆光致抗蚀剂后，通过过蚀刻电极层和绝缘层，形成发射尖端，该过蚀刻是利用蚀刻溶液，使其渗透所述的平面图形并且超出该所述的平面图形，从而通过过蚀刻形成发射尖端，此后，在所述平面图形的位置形成一个柱形栅极，并去除抗蚀剂。

27. 根据权利要求26所述的制造方法，其中，所述位置形成栅极之前，去除所述平面图形周围的抗蚀剂。

多极场致电子发射器件及其制造方法

本发明涉及一种多极场致电子发射器件，该器件能够控制从冷阴极场致发射的电子。尤其是，它涉及一种多极场致电子发射器件，其中，输入信号电压和阳极电流成线性关系，该器件可用于诸如功率放大器、线性放大器和开关电路之类的装置中。

作为现有技术中的多极场致电子发射器件，有一种已在Journal of Applied Physics ，Volume 59，number 2，pages 164 to 169（1990）（应用物理杂志，1990年第59卷2号，第164至169页）中由（Junji ）Ito 发表。图33是现有技术中的多极场致电子发射器件的一个通用示图。

这被称为平面三极管器件。它有一个结构，其中，楔形发射极（阴极）102、柱形栅极103和阳极104依次被制备于石英基片101的表面上。这三个电极是利用光刻工艺形成一微米厚的钨薄膜而制成的。发射极102具有10微米的间距，发射尖端数量为170。发射极102和栅极103之间的距离为15微米。栅极103和阳极104之间的距离为10微米。

当在5×10^{-6} Pa 的真空中测量该三极管器件的电气特性时，发射极发射电流是Fowler Nordheim （F. N）隧道电流。当栅极电压是220V和阳极电压是318V时，得到的阳极电流大约为1. 2mA。对于一个发射极，阳极电流量约为7μA。互导约为0. 1μs。

但是，现有技术中的三极管器件存在很多问题，下面将讨论这些

问题 即，从发射极１０２发射的电子，射向阳极１０４，然而，由于加有正偏压的栅极１０３位于这两电极之间，部分发射电子将流到栅极。因为栅极电流是等于或大于阳极电流，故栅极输入电阻是很小的。也就是说，流到阳极１０４的电子数额（阳极电流除以总发射电流）将减少，导致电气特性下降，因为诸如效率和互导之类的参数是低的。利用现有技术，该数额处于６０％的水平。当控制具有低输入电阻的三极管器件的阳极电流时，为了把输入信号加到栅极１０３，需要一个驱动电路，该电路能够控制诸如大电流和大功率之类的参数。由于这种限制，难以利用现有技术中的三极管器件作为电流放大器和电源开关。

此外，发射极的发射电流是Ｆ．Ｎ隧道电流，它随栅极电压按指数关系增加或减少。结果，阳极电流随栅极输入信号按指数关系变化具有非线性的输入与输出关系的三极管器件，不能应用到诸如线性放大器之类的装置中。

进一步，为了增大三极管器件的互导和改善其性能，需要修改栅极１０３的结构和增大发射极１０２的发射表面面积。但是，如果增大发射表面面积，也会增加流入栅极１０３的电子。结果是，利用现有技术，不能获得高性能的功率放大器。

阴极１０２和栅极１０３是在相同的光刻工艺中制备的。当光致抗蚀剂曝光时，这些电极之间的距离由分辨率决定。实际上，０．８微米是一个极限 而且，随加工几何尺寸变小，偏差增大。该场致电子发射器件的电子发射的阈值电压和该电压的均匀性，大大地依赖于阴极１０２和栅极１０３之间的距离 结果，难以减小现有技术中的三极管器件的阈值电压 即使阈值电压得以减小，仍存在均匀性差的

问题。

场致电子发射器件的阈值电压大大地依赖于阴极102尖端的曲率半径。即，尖端曲率半径越小，阈值电压越低。为了获得一个实用的阈值电压，希望有一个1000Å或更小的尖端曲率半径。然而，采用现有技术，由于光致抗蚀剂的渗透，极限是2000Å。因而一个实用的尖端曲率半径的制备是困难的。

因此，本发明的提出原因是要克服现有技术中存在的问题。其发明目的是提供一种高性能的多极场致电子发射器件，该器件具有大的栅极输入电阻、线性的输入与输出关系，以及大的互导，并提供一种该多极场致电子发射器件的制造方法。

本发明的多极场致电子发射器件的特征是，其至少包括：一个根据场效应发射电子的阴极，一个把电场加到前述阴极的栅极，一个收集发射电子的阳极，以及一个位于前述阴极和前述阳极之间的控制电极，它控制前述的发射电子。本发明的另一个特征是，其至少备有：一个岛状绝缘层，该层在一绝缘平基片的表面上形成；一个阴极，它具有从前述岛状绝缘层伸出的发射尖端；一个在前述平基片表面上形成的栅极，它通常垂直于前述发射尖端的邻近部分；一个在前述平基片表面上形成的阳极；以及一个位于前述平基片表面上的控制电极，它位于前述栅极和前述阳极之间。

此外，本发明的多极场致电子发射器件的特征是，其包括：一个屏蔽电极，它在前述控制电极和前述阳极之间形成，并静电屏蔽前述控制电极和前述阳极；以及一个抑制电极，它形成于前述屏蔽电极和前述阳极之间，并控制前述阳极的二次电子

本发明的场致电子发射器件的制造方法包括一个制造阴极的工艺，

该阴极有一个几乎与平基片表面平行伸出的发射尖端，该工艺至少包含：在前述的平基片表面上淀积和形成一个蚀刻掩模层，在前述的蚀刻掩模层上淀积和形成一个阴极，以及在前述的阴极表面上淀积和形成一个蚀刻钝化层的工序；处理前述的蚀刻掩模层形成一个发射尖端的蚀刻掩模的工序；按照前述蚀刻掩模的形状形成所述的阴极层，从而形成具有发射尖端的阴极的工序。

此外，本发明的场致电子发射器件的制造方法至少包括：在平基片表面上形成蚀刻掩模层的工序；在前述蚀刻掩模层表面上形成阴极层的工序；在前述阴极层表面上形成抗蚀剂层的工序；按前述抗蚀剂层表面的形状处理前述阴极层的工序；利用过蚀刻方法处理前述蚀刻掩模层形成蚀刻掩模的工序；从阴极的较低周边除去前述的蚀刻掩模形成糖形阴极的工序；利用定向粒子淀积形成栅极层的工序；以及处理前述栅极层形成栅极的工序。

本发明的多极场致电子发射器件包括：一个在绝缘层上形成的阴极，该绝缘层位于一绝缘平基片的表面上，该阴极具有多个从所述绝缘层伸出的尖端，一个在所述平基片表面上形成并收集发射电子的阳极；一个在所述阴极和所述阳极之间形成的栅极，它至少在相应于所述发射尖端的一个位置有一开口；以及一个在所述栅极和所述阳极之间形成的控制电极。

本发明的多极场致电子发射器件或许至少包括：一个根据场效应发射电子的阴极；一个把电场加至前述阴极的栅极；一个收集发射电子的阳极；以及一个位于前述阴极和前述阳极之间的控制电极，它控制前述的发射电子 除了前述的阴极、栅极、控制电极和阳极之外，它还包括〔另〕一个控制电极，其位于前述控制电极和前述阳极之间，

一个静电屏蔽前述阳极的屏蔽电极；以及一个在前述屏蔽电极和前述阳极之间形成的抑制电极，其控制前述阳极的二次电子。

本发明的阴极形成于绝缘层的表面上，该绝缘层形成于绝缘平基片的表面上，该阴极具有从前述绝缘层伸出的发射尖端，与发射尖端的形状相应，绝缘层形成为岛状。栅极层中的开口用于使阳极有效地收集从阴极发射的电子。例如，若开口是环形的并在形成于尖端的对应位置，那么流到栅极的电子数量会显著地减少，栅极输入电阻会变得很高。作为发射电流流至环形开口内的结果，栅极电流和控制电流将减小，寄生电流也将减小。

下面描述本发明的实施例。图1是四极场致电子发射器件的一部分的剖视面。该器件中的栅极5和控制电极6是由厚度为1000Å的钼薄膜制成的，它们位于由石英制成的平基片1的表面上。有一个岛状绝缘层2，其厚度为5000Å，由二氧化硅制成，并邻近栅极5和控制电极6。在岛状绝缘层2的表面上，邻近栅极5的电极是阴极3，该阴极厚2000Å，并具有伸出的发射尖端4。在岛状绝缘层2的表面上，靠近控制电极6的电极是阳极7，其厚度为2000Å。

阴极3的结构是这样的：淀积的第一阴极层（3a）为厚度是1000Å的钨（W）膜。淀积的第二阴极层（3b）为厚度是1000Å的钼（Mo）膜。与阴极3相似，阳极7的结构是，淀积有第一阳极层（7a）和第二阳极层（7b）。这四个电极，即阴极3、栅极5、控制电极6和阳极7，依次排列于平基片1的表面上。

阴极3包括多个发射尖端4，它们以5微米的间距排成一行，如此构成发射尖端4，即，使它们沿着与栅极5平行的方向伸出，栅极

5位于平基片1的表面上。如此配置岛状绝缘层2，使之在发射尖端顶尖附近不存在。发射尖端4的水平方向的尖端曲率半径是大约400Å。

如此形成栅极5，使它自行对准阴极3，并在发射尖端4的较低的纵向部分具有一个与发射尖端4几乎相同形状的凸出区域。栅极5和发射尖端4之间的距离（Lgk）由岛状绝缘层2和栅极层5的膜厚决定。它是岛状绝缘层2的膜厚减去栅极层5的膜厚所得的值（Lgk＝4000Å）。根据构成薄膜的最新方法，膜厚控制是很好的。因此，该器件的Lgk的可控性、重复性和均匀性是很好的。

在发射尖端4的顶尖附近，栅极5的宽度大约是2微米。栅极5与控制电极6之间的距离（间隔）是4微米。控制电极6的宽度是8微米。控制电极6和阳极7之间的距离（间隔）约为10微米。栅极5的宽度越小，栅极电流越小，效率越好。此外，阳极7的宽度和表面积越大，电子产额越高。控制电极的宽度越大，互导越大，阳极电流的可控性越大。然而，由于流入控制电极6的电子（控制电流）数量增加，控制电极的宽度应由这些参数之间的平衡决定。理想的尺寸范围是：控制电极6的宽度大于栅极5的宽度，但小于阳极7的宽度。为了增加放大系数（$\mu = c_{CG} / C_{AG}$，其中c_{CG}是栅极5与控制电极6之间的电容，C_{AG}是栅极5与阳极7之间的电容），就意味着要减小控制电极6的宽度和增加控制电极6与阳极7之间的间隔。

图2说明图1所示的本实施例的四极场致电子发射器件的制造工艺。这是在完成主要结构性制造工艺后的状态的常规纵向剖视面。图2（A）表示的该器件的状态是：在平基片1的表面依次分别淀积了绝缘层8、阴极9和蚀刻钝化层10，并已形成了光致抗蚀剂层11

平基片1是一个绝缘的石英基片。绝缘层8、阴极9和蚀刻钝化层10是利用溅射淀积方法依次淀积而成的。绝缘层8、阴极9和蚀刻钝化层10分别由厚度为5000Å的二氧化硅薄膜、厚度为1000Å的钨薄膜和厚度为2000Å的二氧化硅薄膜组成。在阴极3和阳极7构形后，使光致抗蚀剂层11构图。

图2（B）为通过过蚀刻钝化层10制成蚀刻掩模后的该器件的剖视图。过蚀刻方法是：利用HF（氢氟酸）型蚀刻溶液选择性地蚀刻蚀刻钝化层10，使所蚀刻掉的蚀刻钝化层10比由光致抗蚀剂层11所限定的区域还要多。通过将钝化层10从外向内蚀刻得比光致抗蚀剂层11上面的与发射尖端4相对应的区域的曲率半径更多，可以获得具有小曲率半径的发射尖端4的蚀刻掩模12。在本实施例中，光致抗蚀剂层11的曲率半径是3000Å。因此，所产生的5000Å过蚀刻，可获得具有300Å的顶尖曲率半径的蚀刻掩模12。

图2（C）是制成阴极层9并形成第一阴极层（3a）和第一阳极层（7a）后的该器件的剖面图。在去除光致抗蚀剂层11后，具有尖锐的发射尖端的掩模12被用于制造阴极层9。利用干蚀刻法制备阴极层9。在CF₄／O₂＝60／120气流比率的气氛下，施加700瓦射频功率，干蚀刻5分钟。在这段时间内阴极9被过蚀刻，从而得到第一阴极层（3a），它具有顶尖曲率半径为300Å的尖锐的发射尖端。

图2（D）是该器件的一个剖面图，此时，已部分地去除绝缘层8，形成岛状绝缘层2，并暴露出发射尖端4。利用第一阴极层（3a）和第一阳极层（7a）作为蚀刻掩模，用HF蚀刻溶液去除绝缘层8的不需要的部分，形成岛状绝缘层2。在这段时间，发射尖端4

如此暴露出来，即它们从岛状绝缘层2伸出 然后，去除蚀刻掩模12，因为平基片由石英制成，故它几乎没有被蚀刻

图2（E）是该器件的一个剖面图。此时，利用定向粒子淀积的方法已经形成栅极层13。利用溅射作为定向粒子淀积方法，淀积1000Å厚的钼（Mo）薄膜层形成栅极层13。定向粒子淀积方法是沿几乎垂直的方向从粒子源射出粒子并将这些粒子淀积在平基片1的表面上。使用这种方法时，伸出的部分，例如，发射尖端4，成为一个盖，使得淀积在第一阴极层（3a）顶部的钼薄膜层131，淀积在第一阳极层（7a）表面上的钼薄膜层132和淀积在平基片1表面上的栅极层13全部被电气隔离。此外，发射尖端4和与这些尖端有相同形状的伸出部分被如此制备，即它们与发射尖端4的较低的纵向部分自行对准（即使一个电极的位置未校准，另一个电极可如此制备，即，使它的位置与（上述）那一个位置相对应）。可以采用汽相淀积、溅射、电子回旋共振（ECR）、等离子淀积和聚集的离子束作为定向粒子淀积方法。

图2（F）是该器件的一个剖面图。此时，已经去除栅极13、钼薄膜层131和132，并且已经制成第二阴极层（3b）、栅极5、控制电极6和第二阳极层（7b）。利用光刻技术和用光致抗蚀剂覆盖发射尖端4的伸出部分和栅极5之后，采用干蚀刻法蚀刻钼薄膜。

一个制成的多极场致电子发射器件的阴极3的发射尖端4的顶尖曲率半径是400Å。这是因为淀积了第二阴极层（3b），使第一阴极层（3a）有更好的圆度。然而，此圆度引起电场中的发射尖端4的表面积扩大，使得有可能获得大量的和稳定的电子发射 通常，

在第一阴极层（3a）和第二阴极层（3b）使用不同材料的情况下，如果第一阴极层（3a）或第二阴极层（3b）的发射尖端4部分被蚀刻掉，则发射尖端4将变薄，并且膜厚方向顶尖曲率半径将变小，使得有可能得到具有低阈值电压的多极场致电子发射器件。

如果阴极和栅极之间的距离被均匀地缩短，并且将发射尖端的顶尖曲率半径做小，阈值电压将会降低。下面将利用三极场致电子发射器件描述这种情况下的制造工艺。

图3是利用这种制造工艺制成的三极场致电子发射器件的立体视图 该器件的主要元件是：平基片1；岛状绝缘层202；阴极203，它具有从其表面上伸出的发射尖端4；栅极205，它以与发射尖端4自行对准的方式形成，以及在平基片1表面上形成的阳极7。在岛状绝缘层202周围，特别是在平基片1上栅极205的附近是斜面213。斜面213有降低位置的优点，在此位置，从发射尖端4发射的电子流到栅极205，并且还可改善场致电子发射器件的效率

该场致电子发射器件有100个发射尖端，它们有5微米的间距并被排成一行。发射尖端4的顶尖曲率半径是400Å。阴极203和栅极205之间的距离（L_{GK}）是4000Å。在发射尖端（4）的顶尖处，栅极205的宽度是2微米。阴极203和阳极7之间的距离（L_{GK}）大约是10微米。平基片1由#7059玻璃基片（Corning 公司制造）制成。岛状绝缘层202由5000Å厚的二氧化硅薄膜制成，第一阴极层（203a）由1000Å厚的钼（Mo）薄膜制成 第二阴极层（203b）、栅极205和阳极7都是由2000Å厚的钽（Ta）薄膜制成 斜面213的角度大约为10度

图4（A）—4（F）是平基片1的剖面图，它示出图3所示的场致电子发射器件的制造工艺的各主要步骤完成时的状态。图5（A）—5（C）分别是与图4（B）、4（D）和4（E）相对应的平基片1的示意图。下面将描述本实施例的场致电子发射器件的制造方法。

首先，在平基片1表面上形成绝缘层8和阴极层9作为蚀刻层。此后，形成抗蚀剂层11（图4（A））。平基片1是一个具有绝缘特性的#7059玻璃基片。绝缘层8是5000Å厚的二氧化硅薄膜，它是由大气压强的CVD形成的。阴极层9是一个厚度为1000Å的钼（Mo）薄膜，它由溅射形成。通常根据阴极203的形状并利用光刻方法形成抗蚀剂层11。

下一步，按照抗蚀剂层11的形状加工阴极层9，形成暂时的阴极层91（图4（B）和图5（A））。借于使用CF4气体的干蚀刻方法，蚀刻钼薄膜的阴极层9。抗蚀剂层的尖端11a有一个7000Å的尖端曲率半径，它与暂时的阴极91的曲率半径相同。

下一步，借助于过蚀刻绝缘层8（图4（C）），形成蚀刻掩模层81。过蚀刻是这样一种方法，采用各向同性蚀刻方式，在暂时阴极91中所规定的区域内，深深地去除绝缘层8。因为采用各向同性蚀刻手段，从外围向内以等速率蚀刻暂时的阴极91，所以该凸出区域有一个尖锐的形状。结果是，有这样一个特征，即，在该凸出的区域，过蚀刻技术提供一个小的尖端曲率半径。

使用HF型蚀刻溶液作为各向同性蚀刻手段，过蚀刻绝缘层8的二氧化硅薄膜。当把暂时阴极的外周边向内蚀刻1.5微米时，形成倒锥形蚀刻掩模81，它有一个具有300Å的顶尖曲率半径的伸出部分。与暂时阴极的7000Å的尖端曲率半径相比，在锐度方向实

现了20倍增长 在该工艺中，蚀刻平基片1的表面形成围绕蚀刻掩模81的斜面213。绝缘层8的蚀刻速度比平基片1的蚀刻速度快5倍。在发射尖端4的底部形成的斜面213的斜度约为10度。

下一步，把暂时阴极91蚀刻成蚀刻掩模81的形状，形成第一阴极（203a）（图4（D）和图5（B））。当从背面蚀刻时，为了保护，用抗蚀剂层11覆盖暂时阴极91的表面，形成具有与蚀刻掩模81相同的平面形状的第一阴极（203a）。第一阴极层（203a）的发射尖端4的顶尖曲率半径约为300Å。

下一步，蚀刻掉蚀刻掩模81的各侧面，形成岛状绝缘层202，并去除抗蚀剂层11（图4（E）和图5（C））。去除蚀刻掩模81侧面的0.7微米厚度，形成檐形第一阴极（203a），并暴露出突出的发射尖端4。

最后，利用定向粒子淀积形成钽（Ta）电极层后，蚀刻钽层形成第二阴极（203b）、栅极205和阳极7（图4（F））。利用溅射实现定向粒子淀积，形成栅极205，该栅极是由2000Å厚的Ta薄膜制成的。利用定向粒子淀积时，伸出的部分，例如，发射尖端4，成为一个盖，这样在第一阴极（203a）表面上淀积的第二阴极（203b）和在平基片1表面上淀积的栅极205，成为电气隔离的。

与发射尖端4有相同形状的伸出部分如此构造，使它和发射尖端4自行对准。溅射、汽相淀积、ECR（电子回旋共振）、等离子淀积和聚集离子束方法是可用的定向粒子淀积方法中的一些方法 借助于干蚀刻方法加工钽（Ta）薄膜电极层，形成栅极205和阳极7。此时，重要的是用光致抗蚀剂覆盖该层，以使伸出的部分不被侵蚀。

阴极层203是第一阴极(203a)和第二阴极(203b)的重叠结构。顶尖曲率半径约为400Å。如果第一阴极(203a)和第二阴极(203b)使用不同的材料,允许在发射尖端处去掉一个电极,使用剩下的一个电极作为电子发射电极。如果用这种方法把发射尖端做得很薄,则在薄膜厚度方向的顶尖曲率半径将变得更小,从而允许达到更低的阈值电压。

在高真空条件下,测量用这种方法制造的场致电子发射器件。当阴极205接地,阳极电压是常数$V_{ak}=200V$,栅极电压$V_{gk}=60V$时,获得的阴极电流$I_k=4\times10^{-8}$A,在$V_{gk}=100V$时,获得的阴极电流为6×10^{-5}A。此外,阴极203和栅极205之间的寄生电容是在10fF的数量级。

在本实施例中,对于电极,例如,阴极203,所使用的材料是钼和钽薄膜。然而,本发明不限于这些。除此之外,可能使用的其它材料是金属,例如钨、硅、铬、铝和含有这些金属的合金。此外,可以使用具有良好热传导性的基片,例如,陶瓷基片,作为平基片1。例如,可以使用一个绝缘基片,或者使用一个氧化铝基片,该基片具有一个位于导电基片表面上的绝缘体,例如硅基片。另外,绝缘层8和蚀刻掩模81不限于二氧化硅薄膜,也可以使用诸如氮化硅薄膜和氧化铝薄膜之类的薄膜。

为了减小电子发射的阈值电压,也允许用具有小的功函数的材料,诸如钡、钍、铯等,涂覆发射尖端4。此外,阴极203也可由这些材料制备。

为了减小由电子发射产生的噪声,在相同时间借助于激励发射尖端4并产生电子发射,可能产生足量的发射尖端4,并可增加S／N

比率 电子发射并非只能起源于一点，即发射尖端的顶尖 它们可能起源于在该顶尖侧面上设置的附助尖端，该附助尖端将提供相同的效果。另外，借助于把自偏压电阻或者非线性电阻直接连到阴极上的方法，可防止过量电流和噪声。

借助于在阴极7的表面涂覆荧光材料和形成一个光发射显示器或者形成一种诸如能产生X射线的铜薄膜之类的材料，并用电子束激励它，可能产生一个精细的X射线源。当然，对于图1所示的四极场致电子发射器件，同样可以用上述的制造方法。

如上所述，本发明的场致电子发射器件的制造方法具有下面列举的效果：

（1）与借助于过蚀刻阴极层或借助于过蚀刻在阴极层表面上形成的蚀刻掩模层制造阴极的方法相比，有可能制造出具有更小顶尖曲率半径的发射尖端。这是因为，在平基片1表面上形成的蚀刻掩模的蚀刻特性是完全各向同性的。还因为，可使用快速的蚀刻方法，例如，湿蚀刻方法。由于难以用湿蚀刻方法蚀刻诸如钼之类的材料，故也难以借助于过蚀刻这类材料形成发射尖端4。

（2）L_{gk} 通常由岛状绝缘层和栅极的膜厚决定。随着ＬＳＩ（大规模集成电路）加工技术的进步，控制薄膜厚度的能力已变得非常好。使得有可能制成具有好的均匀性和低的电子发射阈值电压的场致电子发射器件。在现有技术中，L_{gk} 的极限是０．８微米。但是，作为本发明的结果，可能制造和获得０．１微米或更低的 L_{gk} 极限。

（3）利用过蚀刻技术，实现了具有小的顶尖曲率半径的发射尖端和低的阈值电压。在现有技术中，顶尖曲率半径的极限是２０００Å。而本发明，可能获得４００Å或更小的顶尖曲率半径。

（4）利用过蚀刻的特点是，象发射尖端4那样的凸出区域具有较小的、尖锐的顶尖曲率半径。相反地，凹的区域是非常平滑的，由于这样的特征，可以利用阴极凸凹区域的优点，防止偶然的电子发射和电极之间的短路。

（5）有可能产生与阴极自行对准的栅极，使电极之间的寄生电容减小，且可高速工作。特别是，由于产生具有低电阻率的第一阴极，〔这种方法〕适用于具有低的线路电阻和较小的线路延迟的高速器件。

（6）图6（A）是采用上述新的四极场致电子发射器件的一种平面四极真空管的通用视图。图6（B）是沿图6（A）中所示的A—A线剖开的剖视图。该平面四极管具有这样的结构，即其中有一平基片1和一个对置的基片14，前者有一个如上所述的四极场致电子发射器件。这两个基片几乎相互平行配置，并沿周边用支架17支撑。一个四极场致电子发射器件密封在由平基片1、对置的基片14和支架17围成的真空层23内。对置的基片14是由石英制成的。在面对真空层的表面上是导电的薄膜，它防止静电电荷。此外，有一个密封口16，当抽空后，在此把真空层23密封。密封口16是通过在由Cr／Au薄膜制成的口内熔化Au和Sn合金来密封的。预先在对置的基片14的表面上形成吸气层18，它是由Al和Ba薄膜合金制成的。在真空层23密封后，用激光加热吸气剂，将它蒸发到真空层的壁上，使其吸气作用还原。

支架17是低熔点的玻璃粉和直径为100微米的玻璃纤维的烧结的混合物　它很好地密封和粘附各基片，并保持真空层23的间隙在100微米。

该四极场致电子发射器件的外引线，即，阴极引线19、栅极引

线20、控制电极引线21和阳极引线22，借助于金属薄膜穿过平基片1和支架17伸出真空层23外部。该平面四极真空管的尺寸是长7mm、宽4mm、厚2.2mm。与现有技术中的热电子发射型真空管相比，它是很小的，是现有管的1/1000或更小。真空层23中的真空度是1×10^{-7}毛或更低。

阳极7是在平基片1的表面上形成的。但是，本发明不限于那样。例如，可在对置的基片上形成阳极。还有，在这种情况下，可以在真空层23内设置控制电极6，这样它将位于发射尖端4和阳极7之间。

图7至图9显示上述四极场致电子发射器件的电特性。图7是使用四极场致电子发射器件的一种阴极接地的电压放大器的电气连接图。前述的四极真空管用标号30代表，它在图7的中央示出。该图示出，阴极3、栅极5、控制电极6和阳极7已被密封在真空层23里面。

使用四极场致电子发射器件的电压放大器的驱动方法如下。即，将阴极3接地并给栅极5加上正偏置栅极电压26（V_{GK}），通过负载电阻28（R_L）给阳极7加上正阳极电压27（V_{AK}），给控制电极6加上控制偏压25（V_{CK}）和串联的输入信号电压24。从阳极7和负载电阻28获得的输出信号电压29（Vout），与输入信号24成比例。

图8是上述四极场致电子发射器件的电子发射特性示意图。这是该四极场致电子发射器件的栅极电流32（I_g）和阳极电流31（I_A）与栅极电压26的关系曲线的测量结果。在这种情况下，在图7的电连接图中，输入信号电压24和控制偏压25均为零伏。栅极电流32和阳极电流31随栅极电压26按指数关系增加，这表明发射电流是F．N隧道电流。阳极电流31比栅极电流约小两位数。

在现有技术的驱动方式中，用栅极电压２６控制阳极电流３１，电功率转换效率不好。这是因为$I_G > I_A$。其次，由于转移特性也是指数的，在线性放大器中这个方法就很难利用。由于这个原因，可以用加在控制电极６上的电压控制阳极电流３１。

图９是上述四极场致电子发射器件的输入和输出静态特性示意图。这是四极场致电子发射器件的控制电流３３（I_C）和阳极电流３４与控制偏压２５的关系曲线的测量结果。在这种情况下，在图７的电连接图中，栅极电压２６是$V_{GK} = 140V$，输入信号电压２４是０Ｖ，阳极电压２７是$V_{AK} = 400V$。尽管在$V_{CK} < 0$的范围内，阳极电流指数性（非线性）变化，而在$V_{CK} > 0$的范围内，阳极电流３４按直线（线性）变化。这就是说，在$V_{CK} > 0$的范围内，阳极电流３４与加在控制电极６上的电压是成比例的。因此，它可用作线性放大器。此刻，控制电流３３是阳极电流３４的１％或更低，形成一个具有极好输入和输出功率转换效率的场效应电压放大器。

由这样一个控制电极６的场效应控制阳极电流３４的机理与已有技术中的热电子发射真空管的栅极相似。这个机理是，借助控制电极６的偏压在控制电极６与阴极３之间形成的电场（偏压梯度）控制阳极电流３４。如果向控制电极６加负电压，而在发射尖端４附近形成一个负电场，则将对向阳极７去的发射电子施加一个排斥力，并将限制到达阳极７的电子数量。

因为从阴极发射的电子具有初始速度，它们将在阳极的方向上猛增。如果处于中间的控制电极具有负偏压，它们的速度将由于负偏压的偏压梯度而减小，并且一些电子将返回阴极。在这种状态下，电子将存留在阴极与控制电极之间，并形成电子云（空间电荷限制区）。

能流向阳极的电子只限于其所带的能量高于控制偏压的那些电子。已经知道，在这样的空间电荷限制区电子的转移会产生很小的噪声电流。与从阴极产生的发射电流波动（噪声电流）相比，该空间电荷的波动是小的。特别是，具有小能量的电子的波动可以忽略不计。只有那些具有很大能量的电子才能引起阳极电流的噪声。现有技术中的三极场致电子发射器件没有上述空间电荷控制区。从阴极发射的大部分电子到达阳极（发射限制区中的电子转移）。因此，发射电流噪声可以表示为阳极电流噪声。

然而，如果对控制电极6加正电压，发射的电子的排斥力的强度将减弱，而阳极电流34将增大。另外，正偏置栅极5所起的作用如同现有技术中的五极真空管的空间电荷栅极的作用，防止在阴极3区域中空间电荷的滞留。如后面所讨论的，在本发明中，为了防止阳极7的二次电子效应，在阳极7与控制电极6之间再增设一个控制电极。

通过调节控制偏压25可恰当地利用线性和非线性区域。利用线性区域起线性放大作用是合适的，如作线性放大器。利用非线性区域起开关作用是合适的。还有，如果栅极电压26变小，提供线性和非线性区的分界线的控制偏压25将向低电压端移动。因此，具有这样的特点，比如，通过设定所希望的栅极电压26可以自由地选择控制偏压25的电压设定范围。然而，如图8所示，在上述四极场致电子发射器件中，栅极电流显著地高于阳极电流，并且流向栅极的寄生电流是无效的。

图10是本实施例的多极场致电子发射器件的阳极静态特性示意图，它是在图7的电连接图中测量 $V_{AK} - I_{AK}$ 静态特性所得到的结果。测量条件是栅极电压 $V_{GK} = 140V$，输入信号电压为 $0V$，控

制偏压25是$V_{CK}=20V$、$40V$、$60V$和$80V$。从图10中可以知道，在本实施例的多极场致电子发射器件中，在$V_{AK}>150V$的范围内，I_{AK}几乎是常数。还有，I_{AK}随V_{CK}成比例地增加。这个阳极静态特性与现有技术的热电子发射五极真空管的相似。这种特性对线性放大器等应用是适合的。因为阳极电阻很大且输入与输出是成比例关系的。

如果在图7中负载电阻是$R_L=5G\Omega$（千兆欧姆），在图10的阳极静电特性图中可画出负载线36。用这样的电路可把作为放大器的基本系数确定出来。即，当控制偏压25是$V_{CK}=40V$，所加输入信号24为$20V$正弦波（$V_{in}=20Sin(\omega t)V$）时，得到的输出信号29为$50V$正弦波（$V_{out}=-50Sin(\omega t)V$）。电压放大率被确定为2.5。当提高频率$\omega$，并作为放大器测量频率特性时，截止频率$\omega_c$为$100MHz$或更高。

图11示出栅极电流I_G、阳极电流I_A和控制电流I_C与控制电压25（V_{CK}）的关系曲线。当$V_{CK}<V_{GK}$时，控制电流I_C是负的。真空中的离子流和基片表面的漏电流可能引起负电流。然而，由于该电流是稳定的，它很可能是栅极之间的表面漏电流。阳极电流I_A相对于控制电压V_{CK}单调地增加。当控制电压很大时，阳极电流将几乎是成比例地随之增加。就是说，找到了可用于转移特性的线性区域。已发现发射电流几乎不随V_{CK}变化，发射电流由栅极电流决定而不受其它电极之偏压的影响。

图12示出控制电压V_{AK}作为参量的阳极特性曲线。阳极电流I_A随阳极电压V_{CK}和控制电压V_{CK}增加并符合下列等式：

$$I_A=K(V_{CK}+V_{AK})^n$$

24

其中 K、a 和 n 都是常数。该特性曲线与热电子发射三极真空管在空间电荷限制区的特性曲线相同。从该相同曲线图可估算出放大系数 μ（$=1/a$）和互导 gm（$=dI_A/dI_{CK}$），当 $V_{AK}=330V$ 和 $V_{CK}=150V$ 时，它们分别是 1 和 $2.6E-10S$。n 值约为 1.3。当 $V_{CK}<V_{GK}$ 时，部分阳极电流有流向控制电流的趋势。

在图 12 的特性曲线中，gm 和 μ 值都是很小的。实际上，分别要求其值为 $1ms$ 或更多和 100 或更大。提高这两个数值有多种方法。然而，特别是对于 gm，增加发射电流是有效的。

为了进一步增大电压放大系数，增大互导和提高频率特性，有必要增加阴极 3 的发射尖端数量或者把栅极 5 的结构设计成这样，即能减少无效的栅极电流量和增加阳极电流。在本实施例中有六个发射尖端 4。然而，如果，例如，尖端数量增加 10,000 倍和发射电流增加到 10,000 倍，那么电压放大系数和互导也将增加到约 10,000 倍，并允许频率特性提高约 100 倍。为了减少无效的栅极电流量，通过使栅极 5 具有较小宽度或使其具有一个带有在发射尖端 4 外突方向上的一个开角的倾斜面，可减小所发射的电子与栅极 5 碰撞的可能性。

在本实施例中，电连接方式是将阴极 3 接地。然而，本发明不限于这种方式，例如，电连接方式可以是将栅极 5 接地。图 13 是一个栅极接地的电压放大器的电连接图，其中使用了本实施例的多极场致电子发射器件，它将栅极 5 接地并向阴极 3 施加负的阴极电压 37。这个连接方式环同于图 7 所示的方式。这是一个容易使用的放大器，因为线性区和非线性区的分界线不随发射电流的数值结果而变化。

如图 14 所示，当发射电流大的时候，为了获得具有小噪声的发

射电流，可采用这样一种驱动方法，即在阴极与栅极之间接入一个自偏压电阻R_{SB}。图15示出这种情况下的阳极特性。一个$2M\Omega$（兆欧）的自偏压电阻R_{SB}与阴极串联接入，以使发射电流稳定。当$V_{AG}=-270V$时，发射电流为$10\mu A$。根据这个曲线图，所得的数值为$g_m=10ns$和$\mu=1.5$。

这些特性概括在表1中。在所列的四极管器件中，A对应图12，B对应图15。

表　　　　1

器　　件		g_m	μ	转移特性
期望的特性值		$>1ms$	>100	线性
四极管器件	A	$0.2ns$	1	近似线性
		$V_{AG}=300V$，$V_{CK}=150V$，$I_E=1\mu A$		
	B	$10.0ns$	1.5	近似线性
		$V_{AG}=300V$，$V_{CK}=-50V$，$I_E=10\mu A$		
三极管器件		$2.0ns$	>100	非线性
		$V_{AG}=300V$，$V_{CK}=120V$，$I_E=1\mu A$		

图16是一个五极场致电子发射器件的示意图，它是向上述的四极场致电子发射器件增加屏蔽电极S。图17为这个五极管的阳极特性曲线，它是在下列条件下测出的：阴极发射尖端数量为$10,000$，$V_{KG}=140V$，阴极电流$I_K=20mA$。$V_{SG}=100V$，$R_L=1K\Omega$。在图17中若施加负载电阻$R_L=80K\Omega$（用虚线示出），

则放大系数是四倍。此时工作点变为$V_1=-40V$。一个采用五极管的器件的特点是阳极电流不波动，因为即使阳极电流有变动，由于屏蔽电极的存在，控制电极附近的电场将不会变动。就是说，阳极电阻r_a将按下式增加：

$$r_a=\Delta V_A\diagup\Delta I_A$$

在下一个实施例中，将说明一个六极场致电子发射器件及其制造工艺。图18（A）、（B）、和（C）分别是一个平面六极场致电子发射器件的示意图，该图的B—B面和C—C面的剖视图。这个器件具有的结构包括控制电极6、阳极7和位于它们之间的屏蔽电极50和抑制电极53。此外，控制电极6和屏蔽电极50分别装备有柱形控制电极64和柱形屏蔽电极65，它们分别在控制电极6和屏蔽电极50的顶部形成。这些柱形电极如此构成，即它们相对于由阴极3限定的平表面倾斜，它们的高度至少比岛状绝缘层2的膜厚度要高些。

柱形控制电极64具有直径为3微米和高度为5微米的圆柱形状。它有10微米的间距。它距发射尖端4约10微米远并位于两个发射尖端之间。柱形屏蔽电极65为宽度为5微米、厚度为3微米和高度为5微米的板状。每个柱形控制电极64按彼此相隔10微米的距离设置。抑制电极53具有5微米的宽度且位于阳极7和屏蔽电极50之间。它离屏蔽电极50的距离约为20微米，它离阳极7的距离约为50微米。

阴极3具有8个间距为5微米的发射尖端 岛状绝缘层2的厚度为5000Å。栅极5以与阴极3对准的方式形成，它离发射尖端4的距离为3000Å，它的端部宽度为2微米，它离控制电极的距离

为4微米。

由于栅极5的电场作用而从阴极3发射的电子，受控制电极6的电场控制，这就限制了到达阳极7的电子数量。屏蔽电极50保持一个固定的偏压，以防止由于阳极7的电场造成的控制电极6的电场波动。抑制电极53可防止由阳极7产生的二次电子返回到控制电极6的方向。图19用于说明这个实施例的六极场致电子发射器件的制造工艺。它示出了在完成各主要制造工序后的器件的纵向剖视面。下面将说明此制造工艺。

首先，在平基片1的表面上依次形成绝缘层8和阴极9。然后，形成光致抗蚀剂层11（图19（A））。平基片1由氧化铝制成。如同氧化铝基片一样，由于陶瓷基片有高的绝缘性和大的热导率，它是用于制备大功率场致电子发射器件的极好基片。除这种基片外，也可以使用GaAs半导体基片和金刚石基片。绝缘层8由5000Å厚的二氧化硅薄膜制成。阴极9由1000Å厚的钽（Ta）薄膜制成。光致抗蚀剂层11是用于形成阴极3的。

下一步，用过蚀刻法将阴极层9制成第一阴极（3a）（图19（B））。过蚀刻采用干蚀刻方式。过蚀刻在气体$CF_4/O_2=120/100$中进行，并加700瓦射频功率保持25分钟。此后阴极9将被过蚀刻至1微米而形成发射尖端4，尖端4有一个曲率半径为300Å的顶尖。

下一步，蚀刻绝缘层8的局部以形成岛状绝缘层2，并除去光致抗蚀剂层11（图19（C））。绝缘层2的形成方法如同在前面的实施例中所述的方法

下一步，柱形构成层56的形成（图19（D）所示）。柱形构成层56由采用涂覆方法形成的厚5微米的光敏聚酰亚胺树脂制成，作为光敏聚酰亚胺树脂，例如，可采用负片型PI-410（由Ube Kosan 公司生产）。显然，除这种型号的有机材料外，无机材料也可以用作柱形构成层56的材料。

下一步，柱形构成层56被光刻而形成控制电极64和屏蔽电极65（图19（E））。如果柱形构成层56由光敏材料制成，它可采用光刻处理。如果它是由一些其它的有机材料或无机材料制成，则采用诸如活性离子蚀刻（RIE）之类的各向异性方法是合适的。

下一步，采用定向粒子淀积形成栅极构成层133（图19（F））。该定向粒子淀积法是溅射，它用于形成薄膜栅极构成层133。该层是由2000Å厚的钽（Ta）膜制成。为使栅极构成层133覆盖住控制电极64和屏蔽电极65，该层被淀积在这些电极一侧。

最后，蚀刻栅极构成层133形成第二阴极（3D）、栅极5、控制电极6、柱形控制电极64、屏蔽电极50、柱形屏蔽电极65和抑制电极53（图19（G））。如果柱形控制电极64和柱形屏蔽电极65由有机材料制成，只有当去除它们之后才能保持高真空状态。除去它们的方法如下所述。首先，用抗蚀剂涂覆平基片1的表面。此刻在柱形控制电极64和柱形屏蔽电极65的顶部上的抗蚀剂厚度比其它区域变得薄一些。然后，用干蚀刻法把抗蚀剂除去，柱形电极的顶部和栅极构成层133显现出来。当栅极构成层133被蚀刻去之后，每个电极的顶部在其开口中显现出来。最后，用溶剂去除这些电极柱。因为用这种方法制造的电极是中空的，并且不能有成为出气

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源的有机材料，故可用〔加热抽真空〕的办法来建立和保持高真空状态。

图20是使用本实施例的六极场致电子发射器件的一个六极真空管的立体图。在这种情况下，六极场致电子发射器件被真空封装在金属壳内。即是，平基片111固定在密封接头的一定区域。而在平基片上设置六极场致电子发射器件。每个电极通过导线162与密封管脚161连接。密封接头160和金属罩163在真空中封接并形成真空层164。为了保持高真空，吸气材料165在罩163的内壁上形成和〔还原〕。

图21是使用上述六极场致电子发射器件的一种阴极接地型电压放大器的电连接图。在图21中部示出了图18所示的六极真空管，其标号为66。它示出：阴极3、栅极5、控制电极6、屏蔽电极50、抑制电极53和阳极7被密封在真空层164里面。阴极3和抑制电极53接地。控制偏压25和输入信号电压24串联加至控制电极6上。阳极电压27通过负载电阻28加到阳极7上。一个期望的正偏压可加到屏蔽电极50上。不过，为了减少供电电源数和导线数，此正偏压可以与栅极5的偏压（V_{GK}）相同。阴极3与抑制电极53的连接和栅极5与屏蔽电极50的连接可以在平基片1的表面上或真空层164的内部实现。尽管如上的电连接是一个六极管，但其管脚数和电源数却与前面已描述的四极真空管相同。

下面将说明该六极场致电子发射器件的驱动方法。首先，假如一个恒定的栅极电极26加在栅极5上，那么恒定量的电子将从阴极3发射出来。若栅极电压26永远不变化，则发射电子数将保持恒定。在这种情况下，阳极电压27也恒定，如果具有直流偏压的输入信号

24加到栅极6上，栅极电流与之成比例地被控制，并且在连接到阳极的负载电阻28放大的信号电压29。控制电极6的电子场效应与前面已述实施例中所述的效应相同。屏蔽电极50将防止由于电压波动引起的控制电极6附近的电场波动。它还有提高阳极电阻和频率特性的作用。抑制电极53防止由阳极7产生的二次电子流向控制电极50的方向。

当在$V_{AK}=300V$，$V_{GK}=160V$，$V_{KC}=60V$和$R_L=1G\Omega$（千兆欧姆）条件下驱动该六极场致电子发射器件时，可得到的电压放大系数$\mu=8$。在这种情况下，互导$g_m=2\times10^{-9}S$。频率特性与上述实施例中描述的四极场致电子发射器件相比提高了1倍这被认为是由于屏蔽电极50对阳极的屏蔽作用所致。

图22示出六极场致电子发射器件的另一种电连接图。图23示出它的阳极特性曲线。该曲线是在下列条件下测出的：10,000个阴极发射尖端，$V_{KC}=140V$，阴极电流$I_K=20mA$，$V_{SK}=160V$和$R_L=1K\Omega$。将图23与图17相比较可以清楚看到，由于抑制电极的存在，阳极电阻进一步增加了，并且甚至V_{AG}在较小数值范围时，饱和特性就显示出来。阳极电阻为$8M\Omega$。

本发明不仅仅应用于上述平面器件。它还可应用到纵向器件。作为一个例子，在本实施例中将描述在硅单晶基片上形成的一个纵向四极场致电子发射器件。

图24是本发明纵向四极场致电子发射器件的总体构成示意图。这个器件主要包括：一个导电的平基片40，它由具有（100）面的n型单晶硅衬底制成。在平基片40表面上形成的阴极41，它具有铅锤状并将纵向的向上突出；第一绝缘层（42）具它形成于平基片

40的表面上，并围绕阴极41的周边开口；栅极43，它形成于第一绝缘层（42）的表面上并围绕阴极41的周边开口；第二绝缘层（44），它形成于栅极43的表面上并围绕阴极41的周边开口；控制电极45，它形成于第二绝缘层（44）的表面上并围绕阴极41的周边开口；以及对置的基片46，其上形成有阳极47，阳极47位于真空层48的对面，而真空层是在控制电极45上面。

由于阴极41是通过各向异性蚀刻平基片40而制成的，它有一个大体为圆锥的形状，其铅轴垂直于平基片40的表面并具有约1.2微米的高度。它的截面顶角约为90°。在本发明中，采用本方法以外的其它制造方法形成的阴极也是可以使用的。例如，阴极也可以是纺锤形。第一绝缘层（42）和第二绝缘层（44）由二氧化硅薄膜制成，其膜厚分别为6000Å和3微米，两个绝缘层的开口直径大致相同，约为3微米。栅极43和控制电极45由钼制成，其膜厚分别为2000Å和3000Å。每个电极的开口直径大致相同，约为1.2微米。平基片40和对置的基片46借助支架彼此粘附；该支架围绕它们的外缘形成。真空层48在它们之间形成。真空层48的厚度为50微米。对于阳极47，则采用透明导电的铝薄膜。

下面说明这个四极场致电子发射器件的工作过程。对于阴极41来说，当正偏压加到栅极43上时，从阴极41的伸出顶尖场致发射出电子，所发射的电子穿过栅极43和控制电极45的开口到达阳极47。然而，能够到达阳极47的电子数量（阳极电流）可由控制电极45的电极控制，由控制电极45的场效应控制阳极电流的机理与第一实施例中描述的相同。因此，在线性区域，控制电极45的电压与阳极电流成比例关系。即是，当控制电极45的电压是大的负值时，

负偏压梯度从控制电极45在阴极41的方向建立，并且发射的电子被反射而返回栅极43的方向。在这种情况下，阳极电流是小的。然而，当控制电极45的电压高时，会产生一个正偏压梯度。大量电子能通过这个电极，从而得到大的阳极电流。

其中形成有10，000个阴极41的本实施例的四极场致电子发射器件的电特性已测出。在阴极接地的电路中，当栅极电压为120V时，得到3mA的发射电流。阳极电流相对于控制电极电压的变化，也就是互导gm＝20μs。流入栅极43的寄生电流是1％或更少，从而得到了所示的那个极好的特性。

还可知道，如果在本实施例的四极场致电子发射器件中形成屏蔽电极和抑制电极以及类似电极，可改善其电气特性。在本实施例中，阳极47是在对置的基片46上形成的。然而，它也可以在平基片40的表面上形成。在这种情况下，控制电极45可没在阳极47与栅极43之间。例如，它可设置在真空层48的中部。另外，为了减少电极之间的〔重叠〕电容以及提高频率特性和压阻（pressure resistance），在薄膜的阴极41基底上进行互连是合适的。以去除过量区域和重叠区域。在这种情况下，使用一个绝缘平基片40

如同本实施例的四极场致电子发射器件。多极场致电子发射器件可以如下方式形成。即：栅极43垂直于从阴极41出来的发射电子的方向。或者栅极43的开口围绕电子流过的通道，这可减少流向栅极43的寄生电流并产生极好的功效。其原因是，当所发射的电子通过栅极43旁边时，它们仅横穿过与栅极43厚度相当的距离。另一个原因是，发射电子与栅极43相撞的几率是很小的，因为它们穿过开口的中心区　横向的多极场致电子发射器件采用这种结构形式是非

常有效的

　　为了增大横向多极管的互导值，例如，有必要这样设计图1所示的四极场致电子发射器件的栅极结构，即应使阴极3的发射表面积较大。但是，如果发射表面积增大，则流向栅极5的电子数也增多。结果，产生一个问题，即难以获得高性能的功率放大。

　　图25是具有环形栅极51的多极场致电子发射器件的放大立体视图。阴极3具有与图1所示结构相同之结构。开口52设在栅极51的与阴极3的发射尖端4的位置相对应的部分。这可减小从发射尖端4发射并穿过开口52的电子形成的栅极电流和控制电流，并允许减少寄生电流和增大输入电阻。

　　开口52不限于图25所示的形状。该结构可以是这样的，即，一个具有开口和相同电偏压的电极围绕发射尖端4形成，并且从发射尖端发射的电子能够穿过开口电极的内部。因此，开口52可以是圆环形或类似矩形。即使形成的开口52不与发射尖端4完全对应，例如，所形成的开口每隔一个与发射尖端4对应，它仍能起到电子发射器件的作用。

　　正如图8所示出的，通过在栅极51中设一开口，可以改善不好的功率转换系数$I_g \geq I_A$。通过设置控制电极可提供一个具有线性输入和输出电气特性的场致电子发射器件。标号61是控制电极，标号7是阳极。在图25中，如同栅极51，控制电极61的结构也有一个开口62，开口62允许发射电流通过。然而，并非一定要求控制电极61具有这样的结构，它也可以是如图1所示的平板电极形状。

　　对于具有图25所示栅极结构形式的四极场致电子发射器件，可能具有图1所示结构所具有的线性输入和输出关系。此外，还可能急

剧减小栅极电流（栅极电流是阳极电流的 1／1 0 或更小）和急剧减小栅极寄生电流。

与上述控制电极 6 1 相比较，图 2 6 是柱形控制电极 6 3 的立体视图。在该图中，柱形控制电极 6 3 在相邻开口 5 2 之间的间距中间形成，控制电极 6 3 的形状可以是圆柱形或矩柱形。

在本发明的多极场致电子发射器件中，电极的个数是可选择的。很自然，它可以是六极场致电子发射器件，例如，可以用图 2 5 所示的栅极 5 1 的结构代替在图 1 8（A）、（B）和（C）中所示的六极场致电子发射器件的栅极 5 的结构。

这就提供了一个如图 1 8 的器件，但其中的栅极 5 被图 2 5 所示的栅极 5 1 结构所替代。在这种情况下，从发射尖端 4 发射的电子将由控制电极 6 的电场控制，到达阳极 7 的电子数量也受到控制。屏蔽电极 6 0 保持恒定电压，用以防止由阳极 7 的电场引起的控制电极 6 的电场波动。抑制电极 5 3 防止由阳极 7 产生的二次电子返回控制电极 6 的方向。

但是，上述的三维栅极结构在制造方面有很多问题。例如，对于薄膜制造工艺来说，间隙控制是困难的。另外，阴极和栅极之间的电场分布是不均匀的，这就限制了 I a／I g 特性。还有，制造工艺要求有四个光掩模步骤，需要复杂的制造技术。由于这些原因，并基于在阴极与栅极间提供一个三维电场分布的目的，希望提供一种具有均匀结构的栅极，并且该结构将允许自行校准（即使某一电极的位置偏离了，另一电极在与那个位置对应的一个位置上形成）。

下面公开的是解决了这些技术问题的多极场致电子发射器件以及该器件的制造工艺 它形成一个极稳定的电极并大大改善了 I a／I g

特性。这是因为该多极场致电子发射器件包括：在绝缘层顶部形成的阴极，所述绝缘层是在绝缘平基片的表面上形成的，该阴极有从所述绝缘层伸出的多个发射尖端；在所述的平基片表面上形成的阳极。它收集发射电子；在所述阴极与阳极之间形成的多个柱形栅极。所述发射尖端位于相邻的栅极之间。所述的栅极形状与阴极上的发射尖端相对应。此多极场致电子发射器件是这样制造的：在绝缘平基片的表面上依次形成绝缘层和电极层，置留（leaving）栅极的平面图形，以及涂覆光致抗蚀剂。此后，让蚀刻溶液流过平面图形。使平面图形以外的区域蚀刻，而形成发射尖端。然后，在平面图形的位置上形成柱形栅极，并除去抗蚀剂。

图27（a）是该新型多极场致电子发射器件。图27（b）是图27（a）沿a—a面的剖面图。图27（c）是图27（a）沿b—b面的剖面图。图27（d）是图27（a）中的器件的部分立体视图。在该器件中，阴极303、栅极305和阳极307位于由石英制成的平基片表面上。阴极303由在二氧化硅岛状绝缘层302表面上的薄膜（例如，厚度为2000Å）制成。突出的发射尖端在阴极303中形成。阴极303可由几层薄膜制成（例如，在钨薄膜顶面设置钼薄膜）。发射尖端是这样一种结构。即它伸向栅极的方向并平行于平基片1的表面。在发射尖端4的顶尖区没有岛形绝缘层302。发射尖端4的水平方向的顶尖曲率半径是400Å或更小。

栅极305是这样形成的，即它与阴极303校准。其五角柱形的在阴极303方向上的尖角9，例如，具有60至90°的角度发射尖端4在与栅极305相邻的间隔中形成。因此，在发射尖端4附近的电场分布是横向对称的 如果栅极305的五角柱形高度G做

得比阴极303还高，则在发射尖端4区域的电场分布横向对称，同时纵向是基本均匀的。结果，由于阴极303与栅极305之间电场的作用，从发射尖端4发射出来的电子将通过栅极305之间的相邻间隙，并以有效的方式到达阳极307。这将允许明显减小流入栅极的寄生电流。也就是说，Ia／Ig特性（功率转换率）呈现出明显的改善。

栅极305的结构不限于已有的五角柱形。只要柱形能够在发射尖端4周围形成对称电场，并使发射的电子有效地到达阳极307即可（例如，它可以是三角柱形或具有弧形背的柱形）。

在这个实施例中，已经公开了一平面三极场致电子发射器件。但是，采用四极管和五极管等多极场致电子发射器件也能完成本发明。

在图27中，标号71是栅极的互连部分。下面对每个部分的尺寸给出一个例子。栅极305之间的距离A是3微米。栅极305的五角柱形的侧边B是5微米。侧边C是7微米，栅极305与阴极303之间的间隙D是1．5微米，岛形绝缘层302的厚度E是0．5微米，阴极303的厚度F是0．1微米。

下面从整体上说明上述本发明的器件的制造工艺。图28、29和30说明各制造步骤。首先，如图28（a）中的横截面图所示，在基片1的表面上用热化学汽相淀积（CVD）法形成二氧化硅薄膜311。基片1是由石英玻璃等材料制成。然后，用诸如溅射方法在二氧化硅薄膜311顶部形成钨层312。但是，制备此层的材料不限于钨，例如，它可以是诸如钽之类的材料　此后，如图28（b）中所示，置留具有栅极柱形形状的抗蚀剂孔313，并形成抗蚀剂层314　图28（c）示出图28（b）中沿b－b面的剖面。其中

标号与图28（a）、（b）中的相同。当采用CF₄气体等蚀刻时，存在于抗蚀剂孔313中的钨层315被蚀刻掉。如图29（a）所示，在图28（c）中的二氧化硅层316显露出来。

然后，使用HF型蚀刻溶液蚀刻图29（a）中的二氧化硅膜316。当该膜被过度蚀刻之后，得到了在图29（b）中由二氧化硅膜311的剖面示出的倒圆锥。此后，当用CH₄型蚀刻溶液蚀刻钨膜312时，钨的蚀刻过程沿图29（c）所示的虚线317和318进行，其沿c—c面的剖面如图29（d）所示。这就形成了阴极发射尖端319。对于本发明的方法，流出抗蚀剂孔313的蚀刻溶液从抗蚀剂孔313的两侧沿该孔的形状过蚀刻钨膜，作为形成的阴极的一部分的发射尖端319的顶尖是尖锐的。此外，该顶尖的位置与相邻的抗蚀孔313是等距的。结果，在该制造工艺中，形成的发射尖端319可能总是位于相邻抗蚀剂孔313的中间，虽然，抗蚀剂孔313的位置也许有误差。再者，由发射尖端319和栅极形成的电场分布总是横向对称的。也就是说，可以这样形成阴极和栅极，即，使它们自行校准。

此后，采用汽相淀积或溅射方法使钼等用于形成栅极的材料成膜，从而形成钼膜321和322，如图30（a）中的剖面所示。对于钼膜321，其平面形状与栅极相同，后者具有与抗蚀剂孔313相同的形状。根据汽相淀积或溅射的工艺条件，形成的钼膜321的高度大于钨膜312是可能的。当去除抗蚀剂层314之后，结果将如图30（a）和30（b）所示　将形成的阴极和栅极如图27（c）所示。

关于本发明中阳极的形成，当虚线317的区域被蚀刻后，该区

域通过图29（　　）所示步骤中的过蚀刻形成。钨膜320可用作阳极。另外，该阳极可单独制备。不过，在这种情况下，钨膜320也可用作多极场致电子发射器件的控制电极，或者被除去，如果它不是必需的。

栅极互连部分71是预先采用光掩模制备的。因此，对于这个制造工艺，可能采用两个光掩模步骤来实现，一个光掩模步骤用于使栅极互连部分构图，另一个光掩模步骤用于形成如图28（b）所示的抗蚀剂膜。

栅极互连部分的位置可设在所期望的地方。因此，如果它靠近阴极形成，栅极与阴极之间的电场将增强，从而提供一个具有极好的电场的器件。

在上述制造工艺的图30（a）的步骤中，当采用真空淀积或溅射形成钼膜时，有时在钼膜321和钼膜322之间会形成钼桥，如图31所示。由于这对于栅极的形成是不好的，故制造工艺应是一种不形成钼桥323的工艺。

下面一个实例示出这样的制造工艺。图32（a）是图28（c）的一部分的放大的剖视图，它示出同样的制造步骤。当栅极预先在基片1上形成时，与抗蚀剂孔的形状相对应的互连部分图形325也被制成（该中间连接部分的材料可以是，例如，铝，但也可用其它一些材料）。

在这种条件下，当二氧化硅层311被过蚀刻之后，如图32（b）所示，互连部分显露出来。因此，如图32（c）所示，可用真空淀积或溅射方法，在互连部分图形325顶部形成薄铝膜326标号327是指形成在抗蚀剂层314顶部的铝层

下一步，过蚀刻钨层312之后（图32（d）），用氧等离子体等去除围绕抗蚀剂孔328周边的抗蚀剂层314（图32（e））。然后，用真空淀积或溅射方法形成栅极金属329，它是用作栅极的材料（它可以是铝或钼）（图32（f））。此后，去除抗蚀剂（图32（g））。当用这个制造工艺形成栅极时，上述桥是难以形成的，因为抗蚀剂层14的周边被去除了。

本发明的效果

由于本发明有如上所述的组成，它也有下列显著的效果：

（1）由于控制电极的电压与阳极电流成线性关系，输入和输出转移特性是线性的。而且，阳极电阻很大。结果，它可用在线性放大器中，而采用现有技术是有些困难的。

（2）流入栅极的寄生电流明显地减小了。从电流消耗的观点看，它是一种具有有效的线性放大效应的场致电子发射器件。

（3）由于控制电极的输入电阻很大，它可用在场效应放大器或开关器件中。

（4）与现有的热电子发射真空管相比，它控制的电流、电压和功率相同或更好。此外，它是很小的。

（5）由于可用栅极电压控制互导和转移特性的线性程度，即使采用相同的器件，特定的参量也可容易地形成不同的电路。

（6）在器件的构形方面有很大的自由度，以适应其应用，如具有较好频率特性的器件、具有极好的效率的器件或者能够控制大和小电源的器件

附图说明

图1是一种四极场致电子发射器件的组件的立体视图。

图 2 是图 1 所示四极场致电子发射器件的制造工艺步骤示意图

图 3 是展示本发明的实施例的新型四极场致电子发射器件的局部放大的立体视图。

图 4 是图 3 所示四极场致电子发射器件的制造工艺的各步骤的示意图（纵向剖视图）。

图 5 是图 4 所示制造步骤的示意图。

图 6 是使用图 1 所示的四极场致电子发射器件的一种平面四极真空管的示意图，以及由 A－A 表示的区域的纵向剖视图。

图 7 是使用四极场致电子发射器件的一种阴极接地器件的电连接图。

图 8 是图 7 所示器件的电子发射特性曲线图。

图 9 是图 7 所示器件的输入和输出静电特性曲线图。

图 1 0 是图 7 所示器件的阳极静电特性曲线图。

图 1 1 是四极场致电子发射器件的栅极电流、阳极电流和控制电流与控制电压的关系曲线示意图。

图 1 2 是四极场致电子发射器件的阳极特性曲线示意图。

图 1 3 是另一种四极场致电子发射器件的电连接图。

图 1 4 是四极场致电子发射器件的另一种电连接图。

图 1 5 是在图 1 4 的电连接状态下的阳极特性曲线。

图 1 6 是五极场致电子发射器件的电连接图。

图 1 7 是在图 1 6 的电连接状态下的阳极特性曲线。

图 1 8（A）是六极场致电子发射器件的示意图，图 1 8（B）和（C）是该六极场致电子发射器件的剖视图

图 1 9 是图 1 8 所示的六极场致电子发射器件的制造工艺步骤示

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意图。

图20是使用六极场致电子发射器件的六极真空管的立体视图。

图21是该六极场致电子发射器件的电连接图。

图22是该六极场致电子发射器件的另一种电连接图。

图23是图22所示器件的阳极特性曲线图。

图24是纵向四极场致电子发射器件的剖视图。

图25是四极场致电子发射器件的立体视图，其中栅极和控制电极具有开口。

图26是一个实施例的立体视图，其中图25所示的控制电极是柱形电极。

图27（a）是本发明的另一实施例中示出的三极场致电子发射器件的示意图。

图27（b）是图27（a）的沿a—a面的剖视图。

图27（c）是图27（a）的沿b—b面的剖视图。

图27（d）是该器件的立体视图。

图28是说明图27的三极场致电子发射器件的制造工艺的工艺步骤示意图。

图29是说明图27的三极场致电子发射器件的制造工艺步骤的示意图。

图30是说明图27的三极场致电子发射器件的制造工艺步骤的示意图。

图31是说明图29和30所示制造工艺中形成桥的示意图

图32是说明图29和30所示制造工艺中如何不形成桥的示意图

图33是现有技术的三极场致电子发射器件的示意图。

标号含义注解

    1. 平基片

    2. 岛状绝缘层

    3. 阴极

3a. 第一阴极

3b. 第二阴极

    4. 发射尖端

    5. 栅极

    6. 控制电极

    7. 阳极

7a. 第一阳极
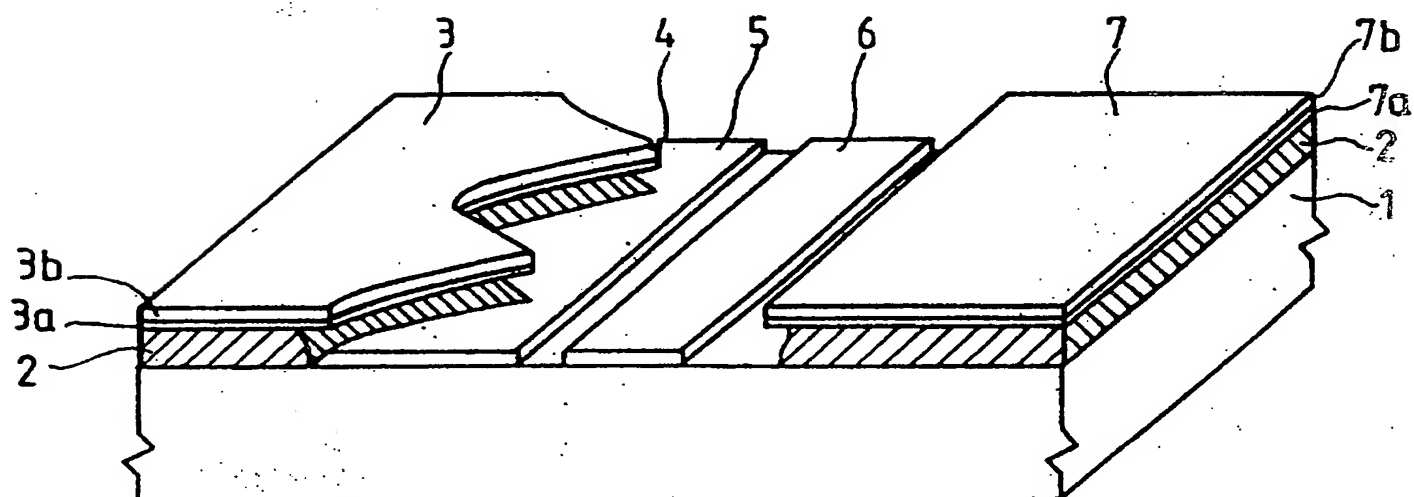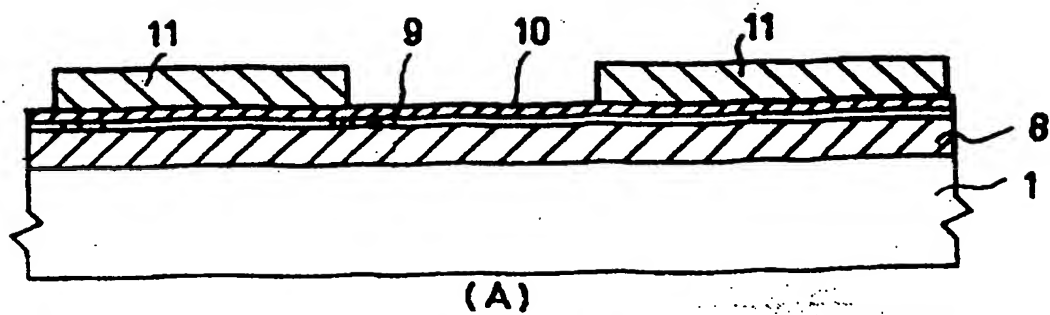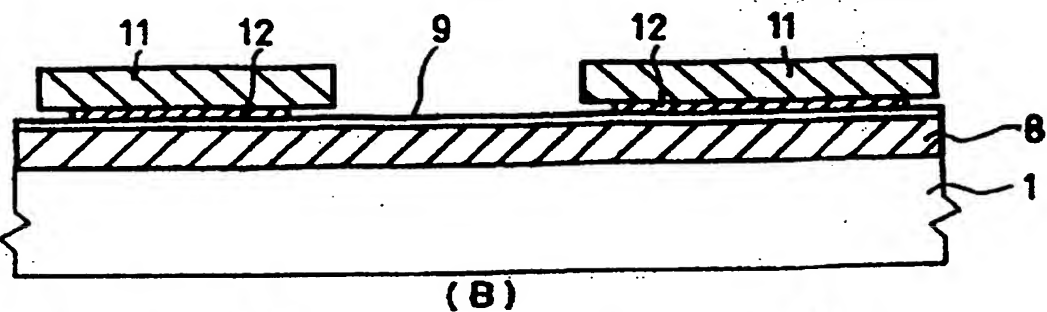
7b. 第二阳极

图 1

图 2(A)
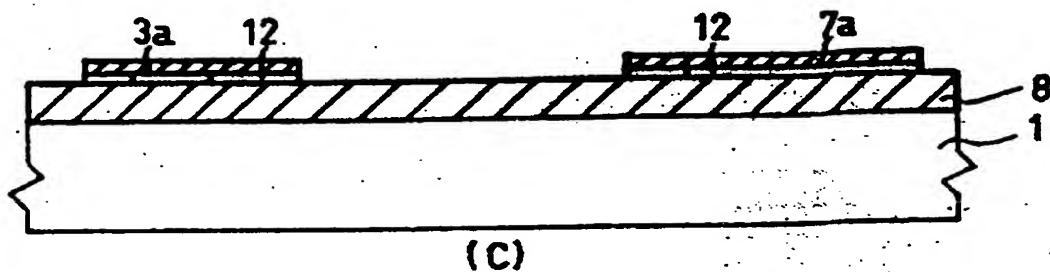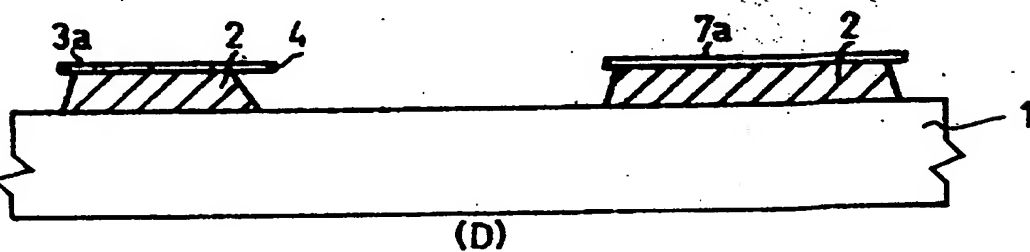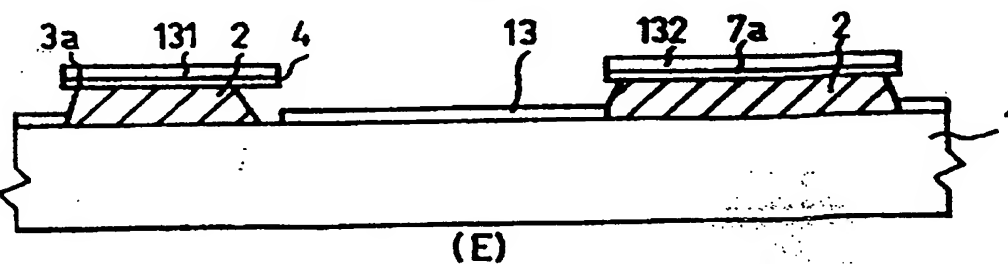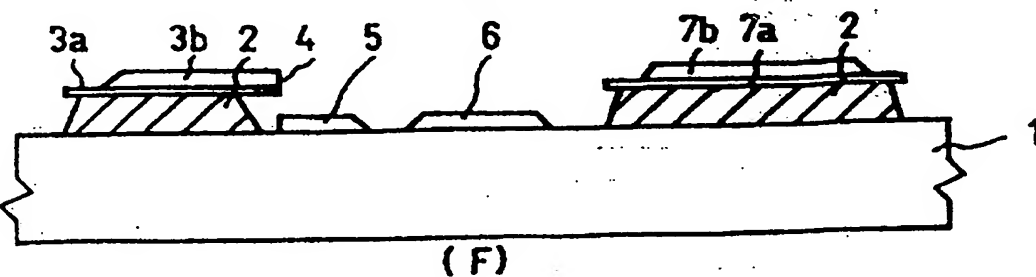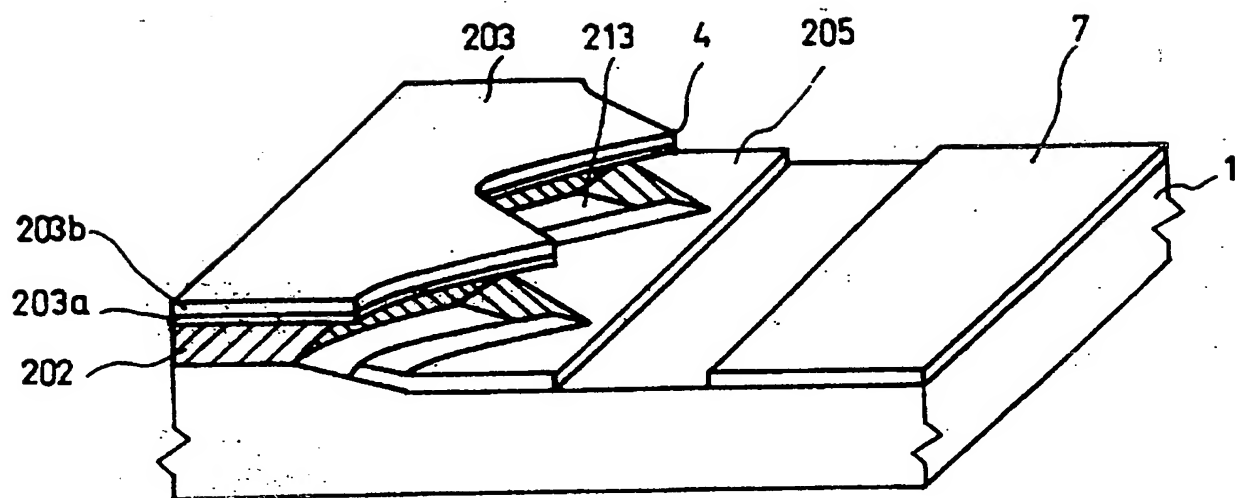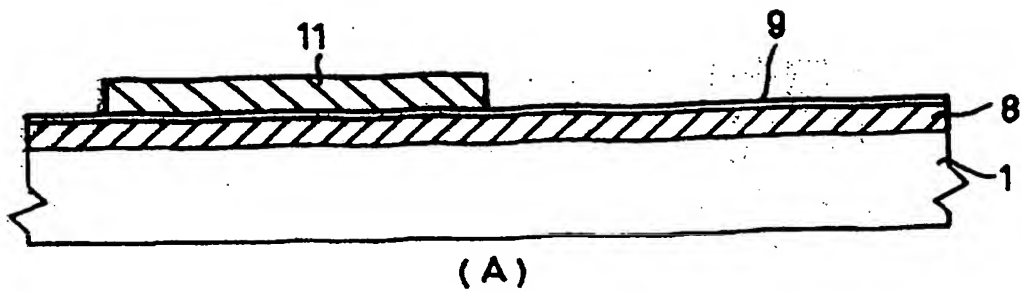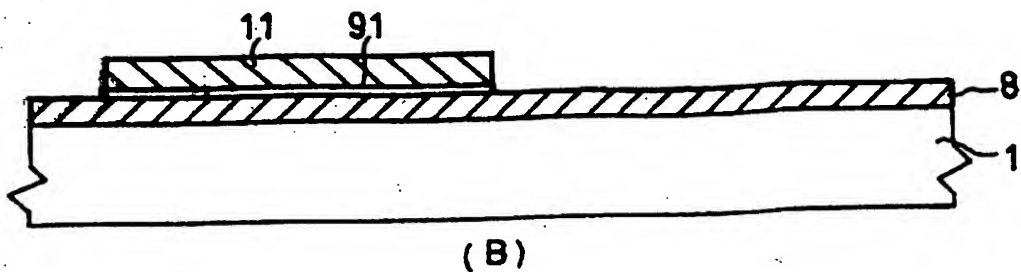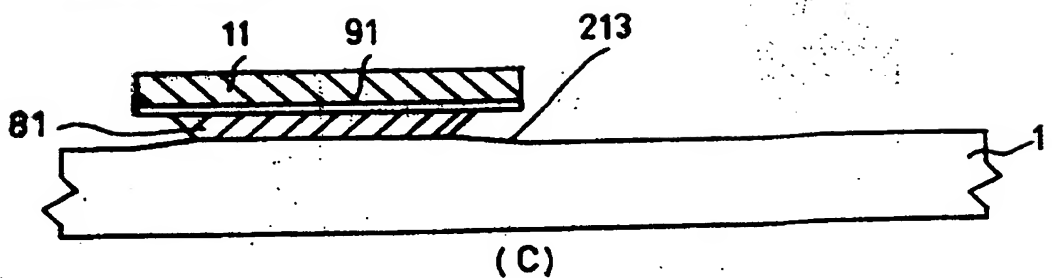
11　　　　9　10　　　　11

8

1

(A)

图 2(B)

11　12　　　9　　　12　11

8

1

(B)

图 2(C)

3a　　12　　　　12　　7a

8

1

(C)

图 2(D)

3a　　　2　4　　　　7a　　2

1

(D)

图 2(E)

3a　131　2　4　　13　　132　7a　2

1

(E)

图 2(F)

3a　　3b　2　4　5　　6　　7b　7a　2

1

(F)

图 3

图 4(A)

（A）

图 4(B)

（B）

图 4(C)

（C）

图 4(D)

（D）

图 4(E)

（E）

图 4(F)

（F）

图 5 (A)

(A)

图 5 (B)

(B)

图 5 (C)

(C)

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(A)

図 6(A)

(B)

図 6(B)

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图 1

图 8

図 9

图 10

图 11

図 12

图 13

图 14

图 15

图 16

图 17

図 18(A)

図 18(B)
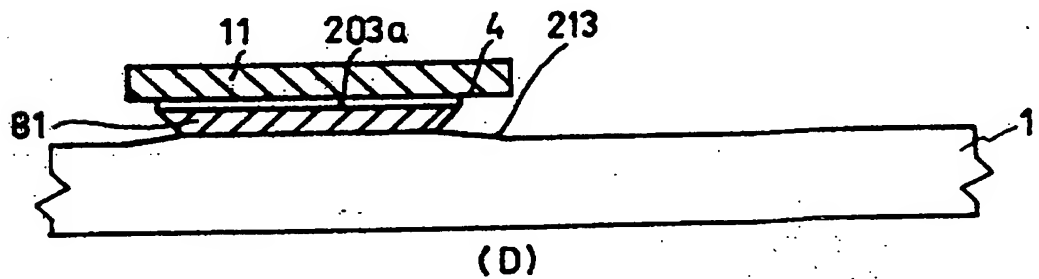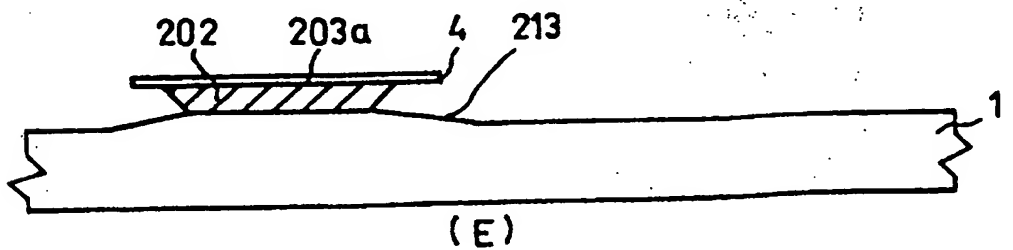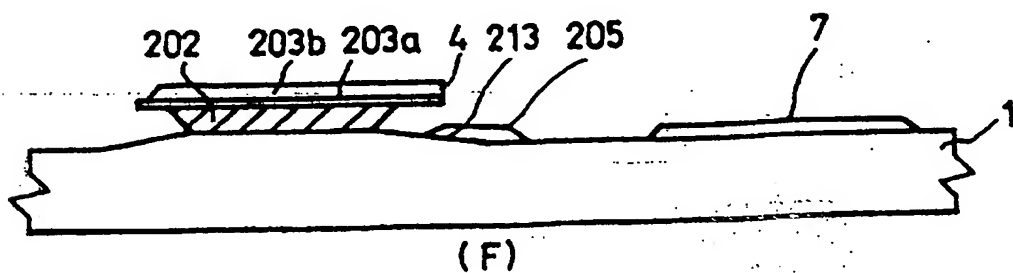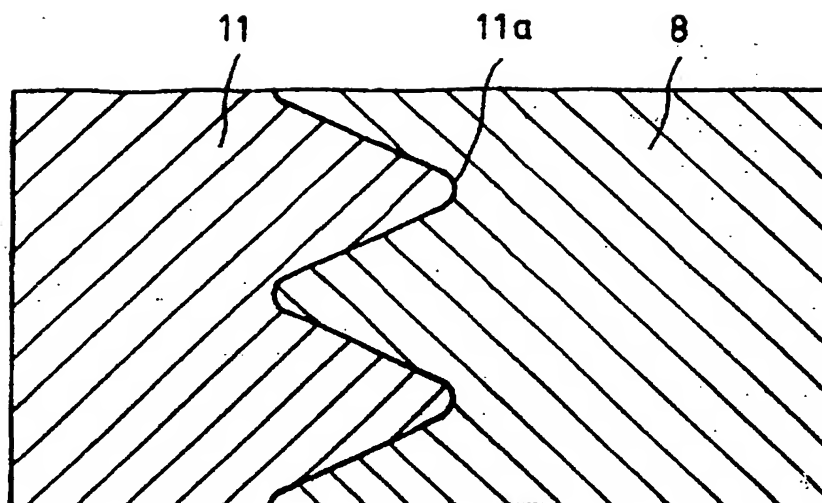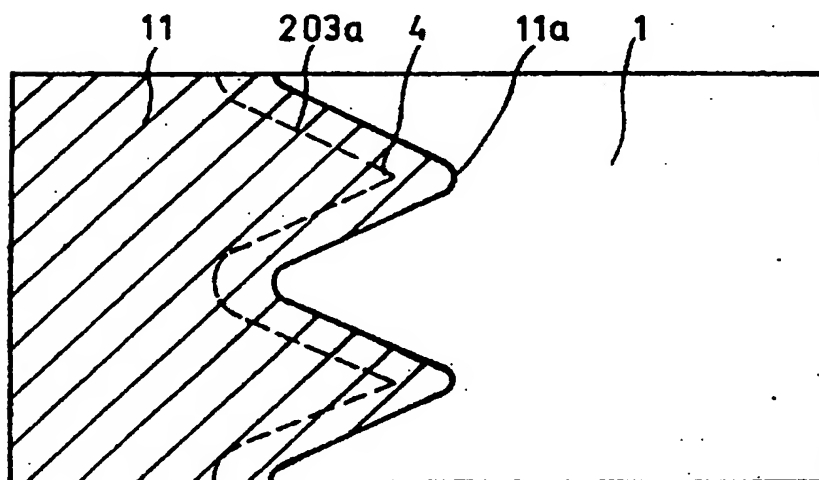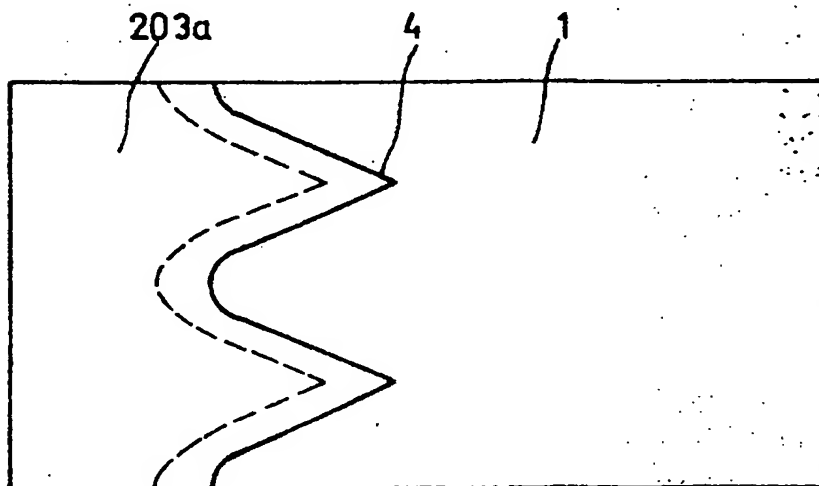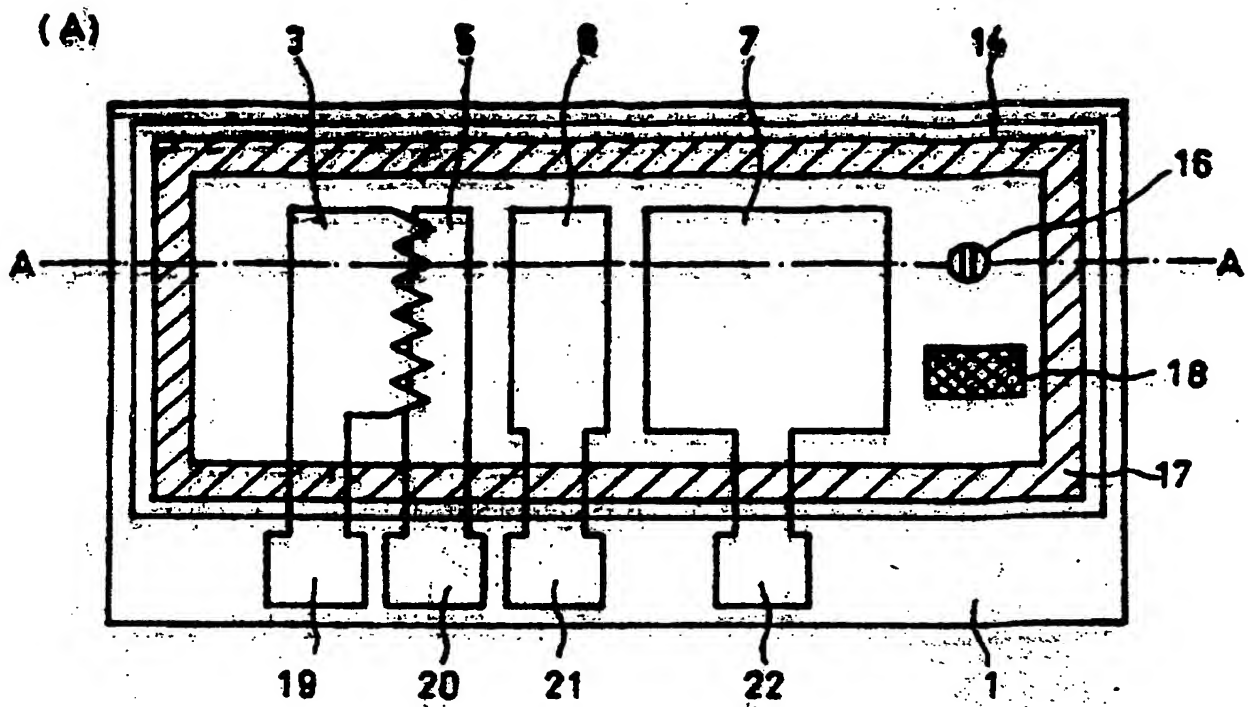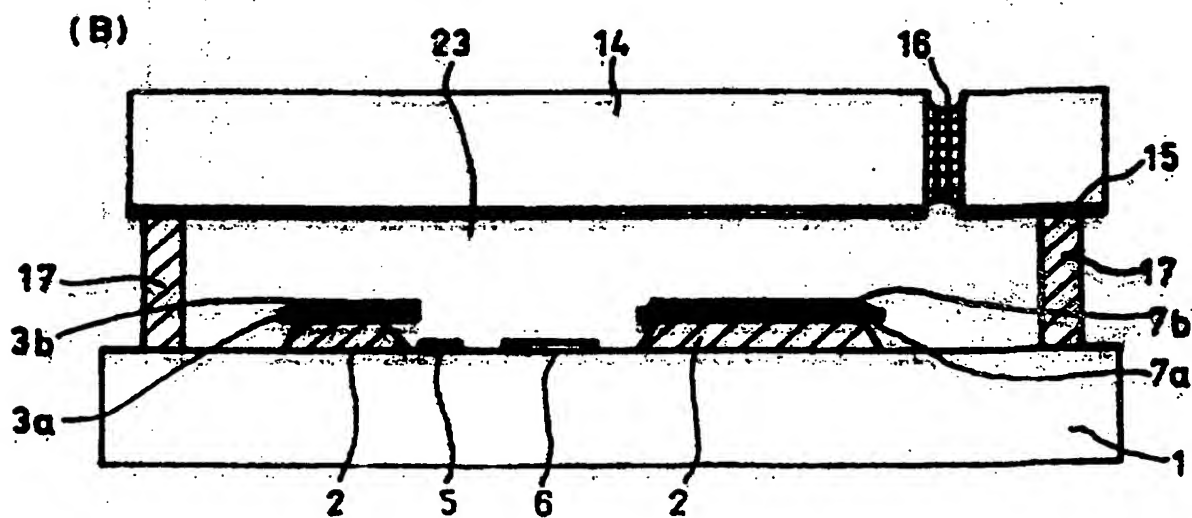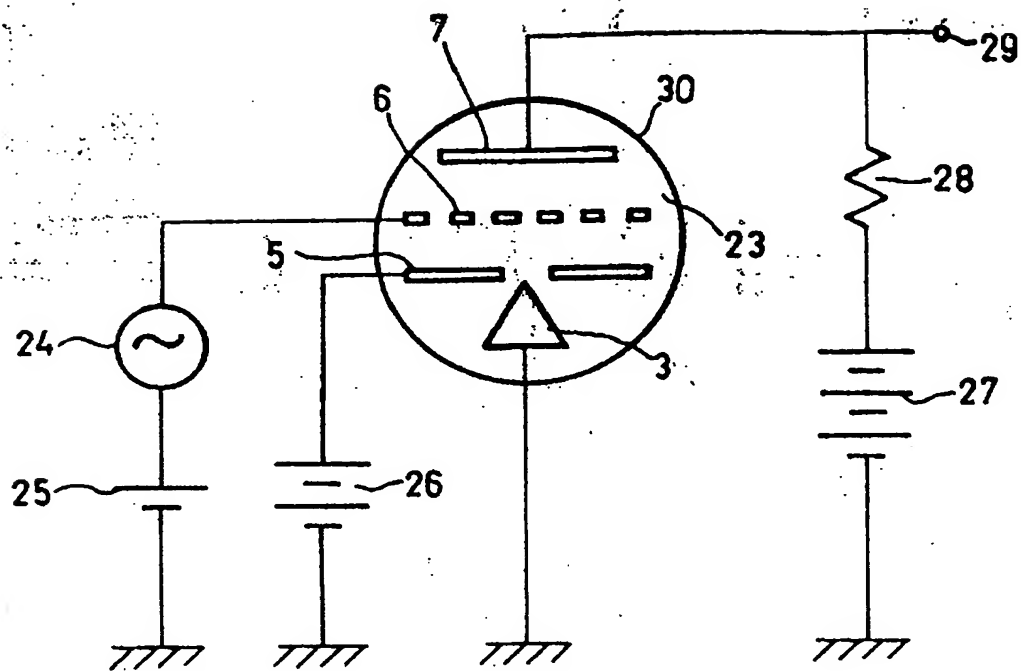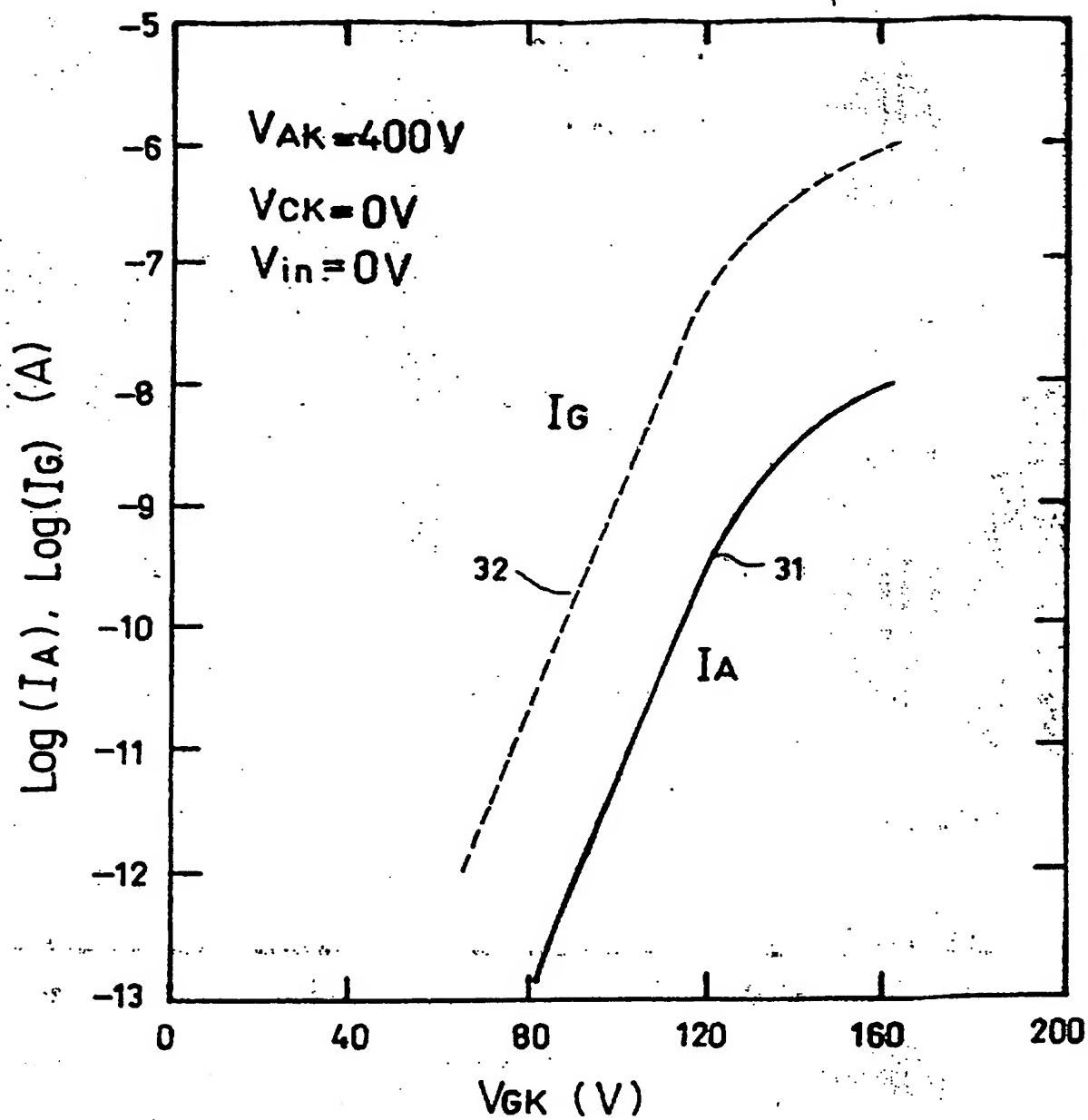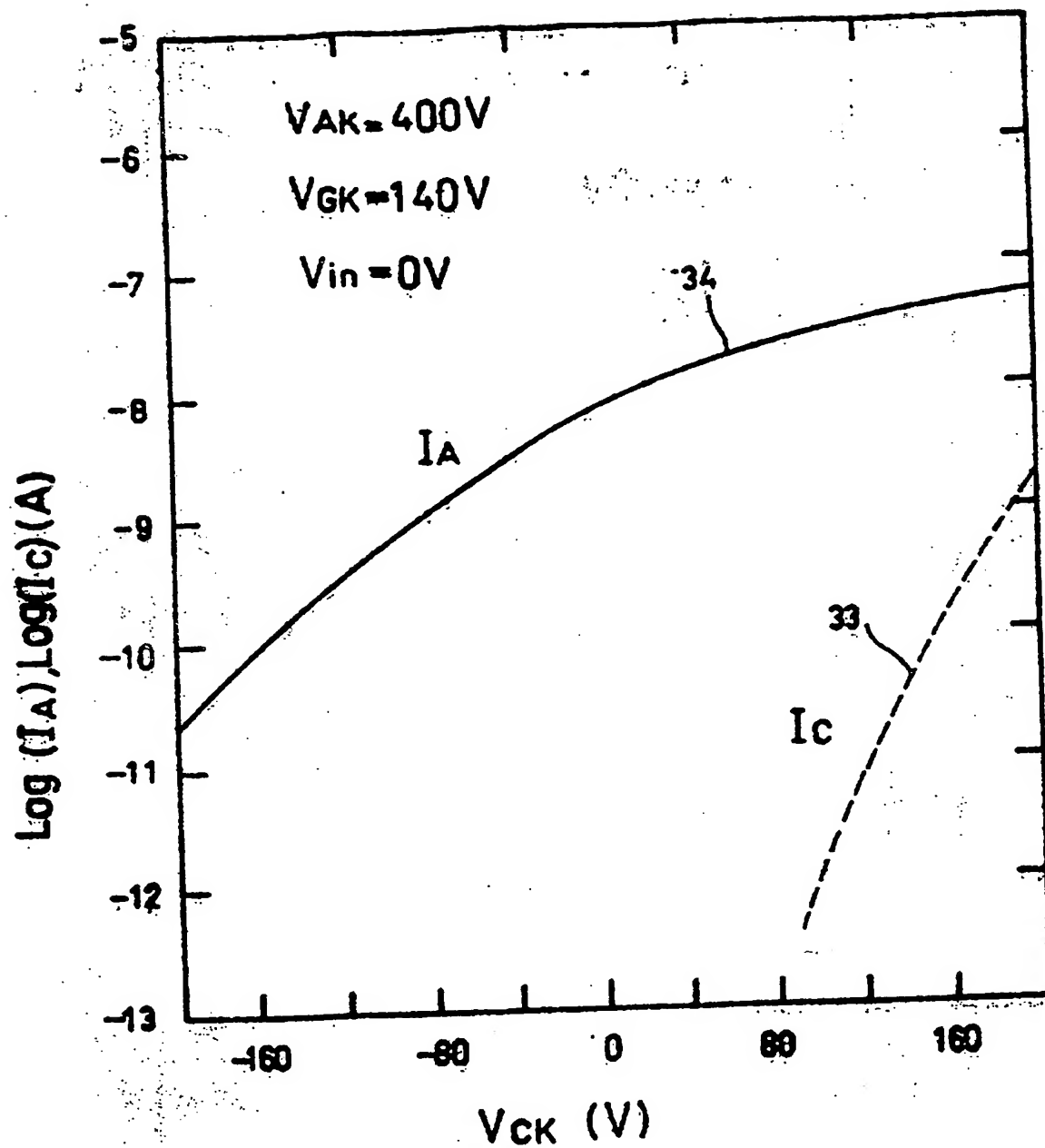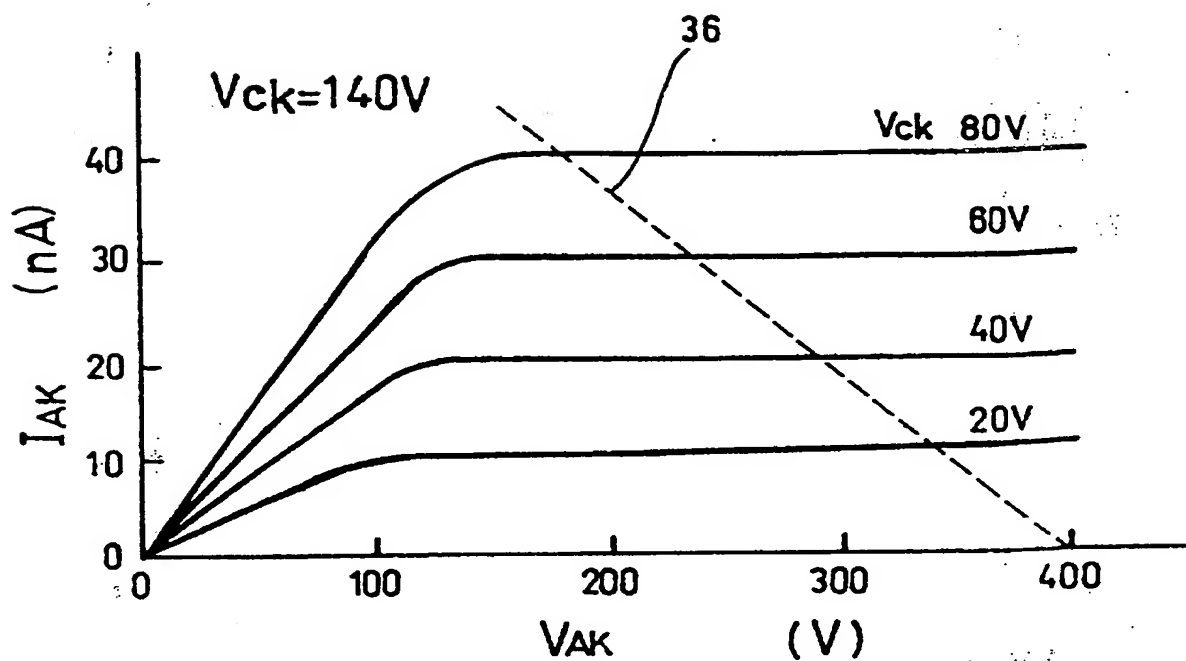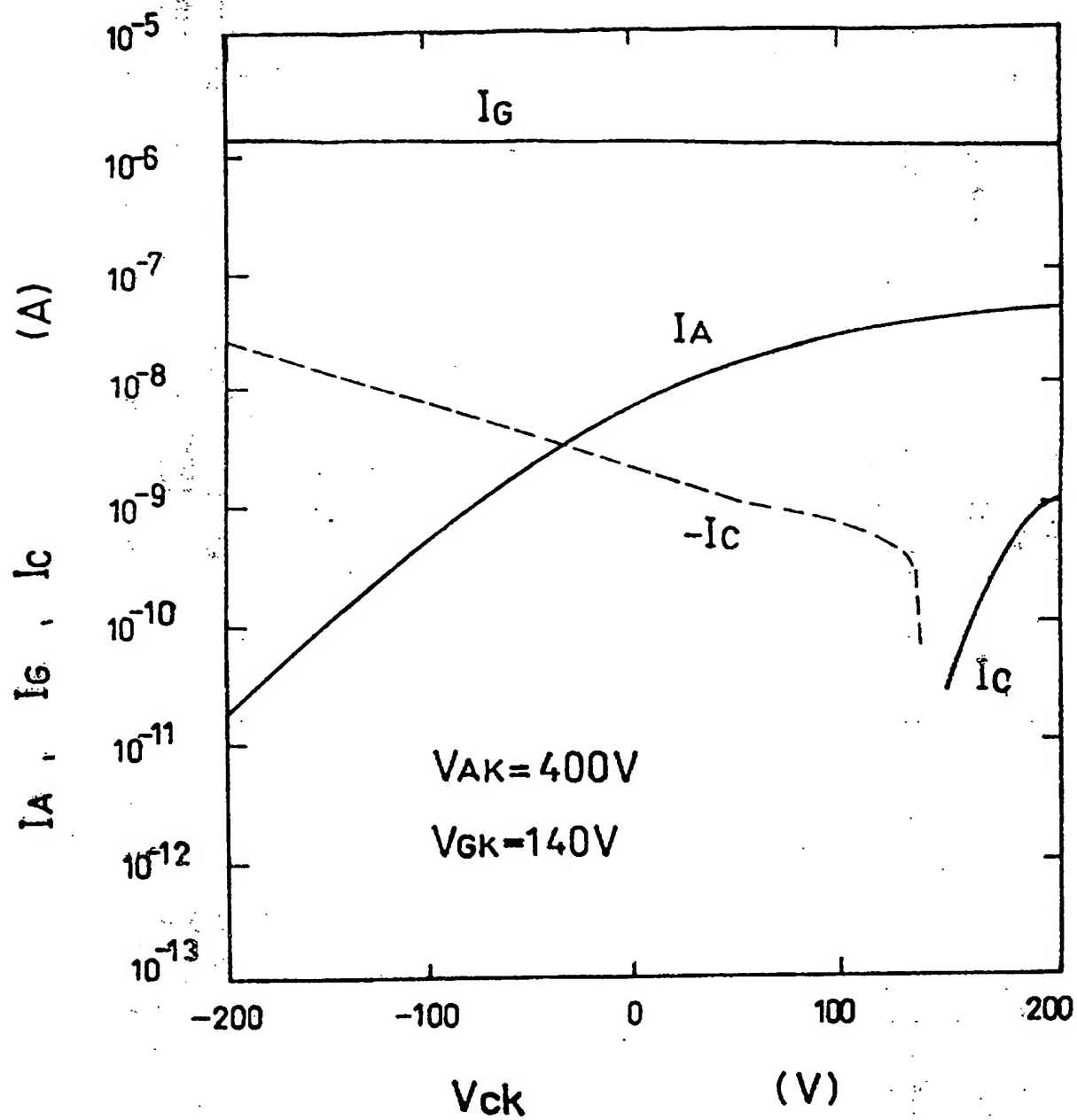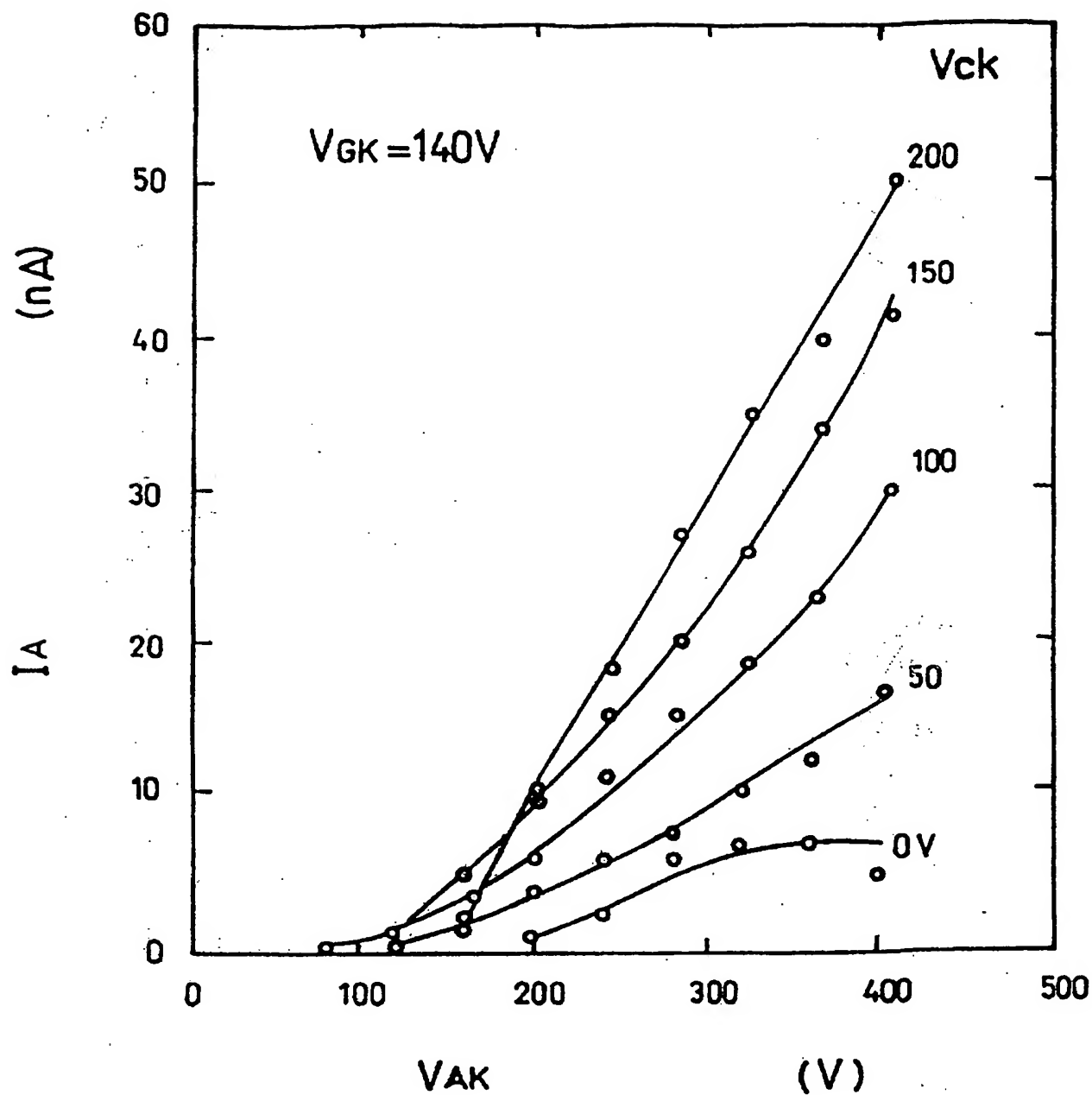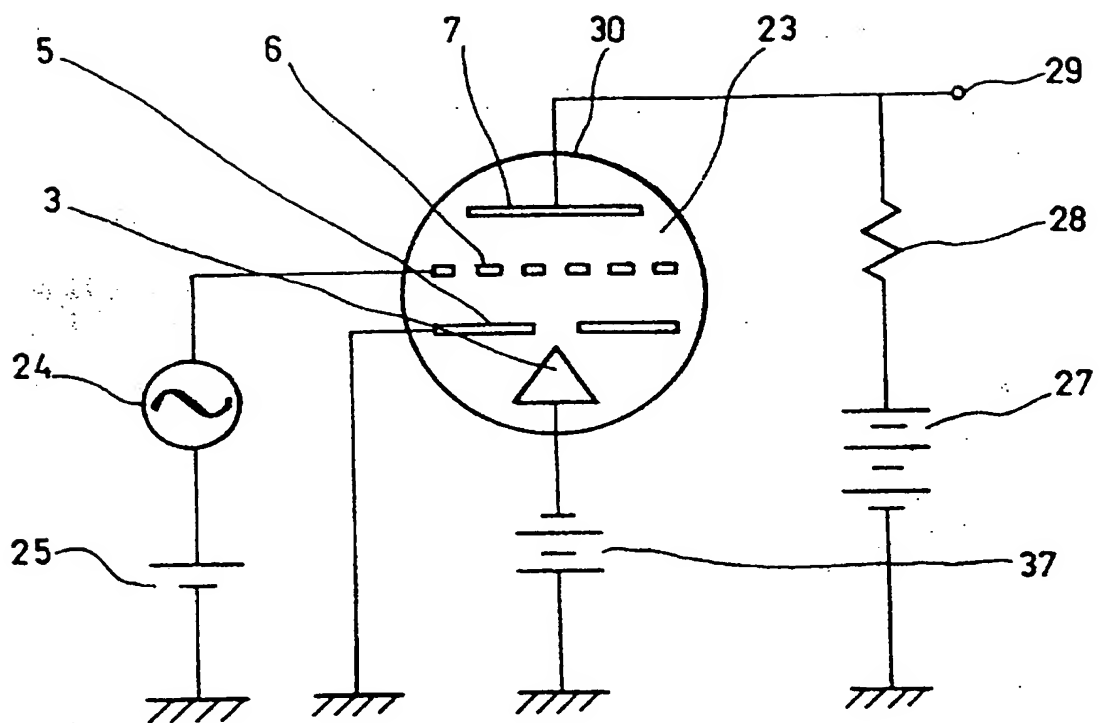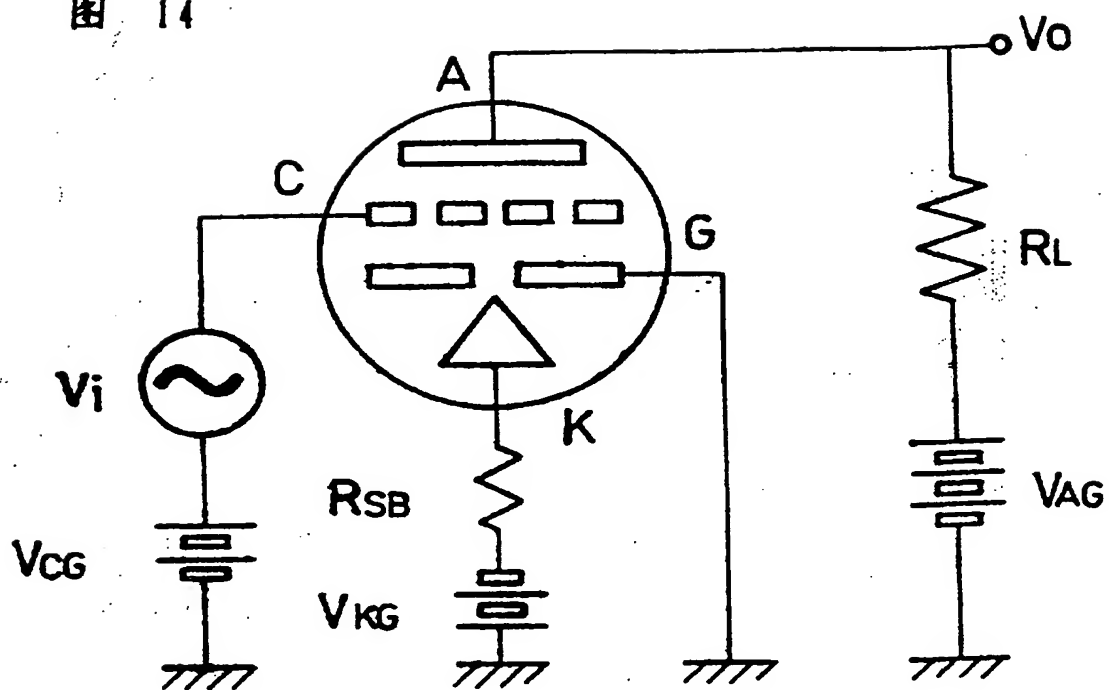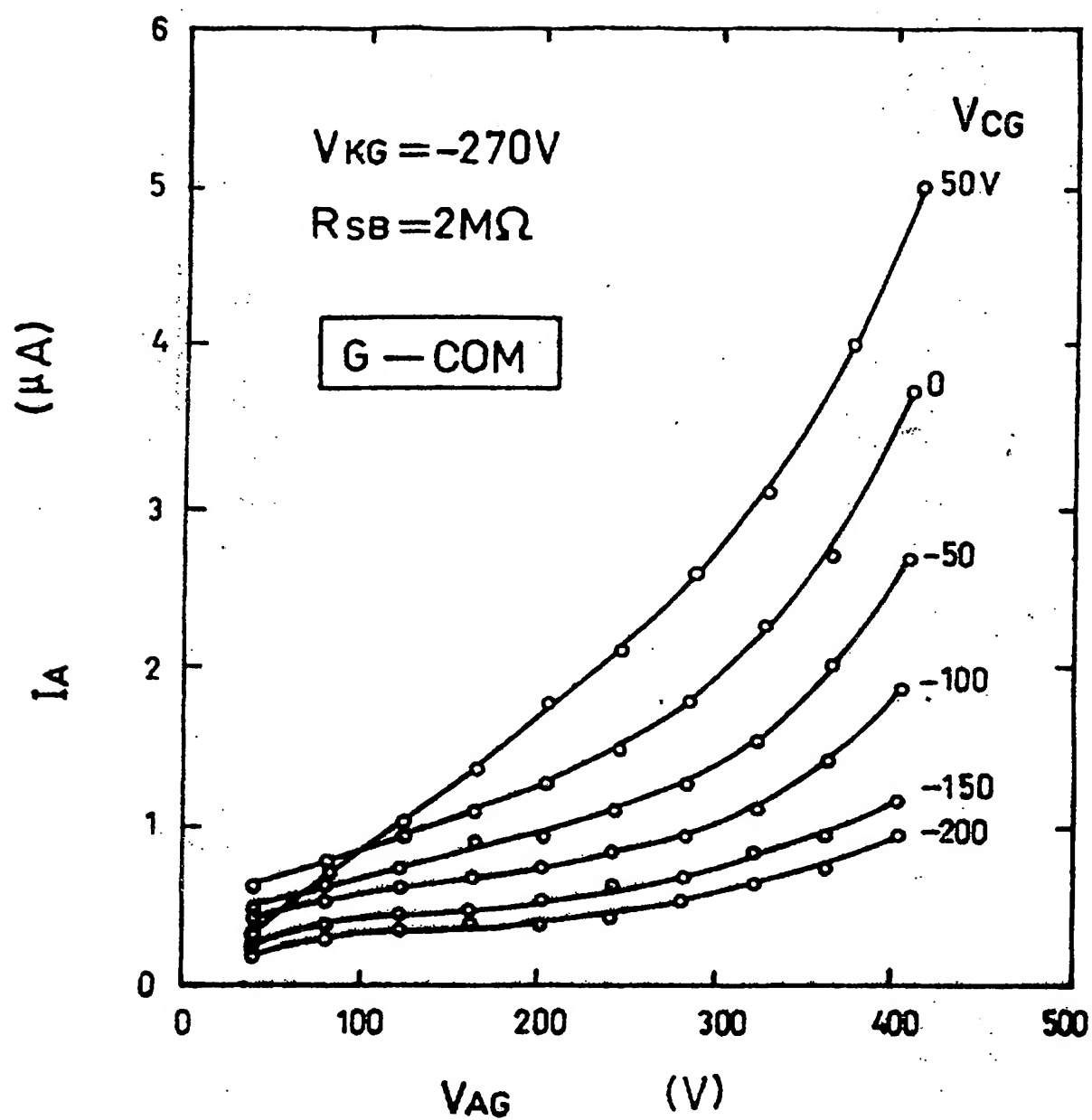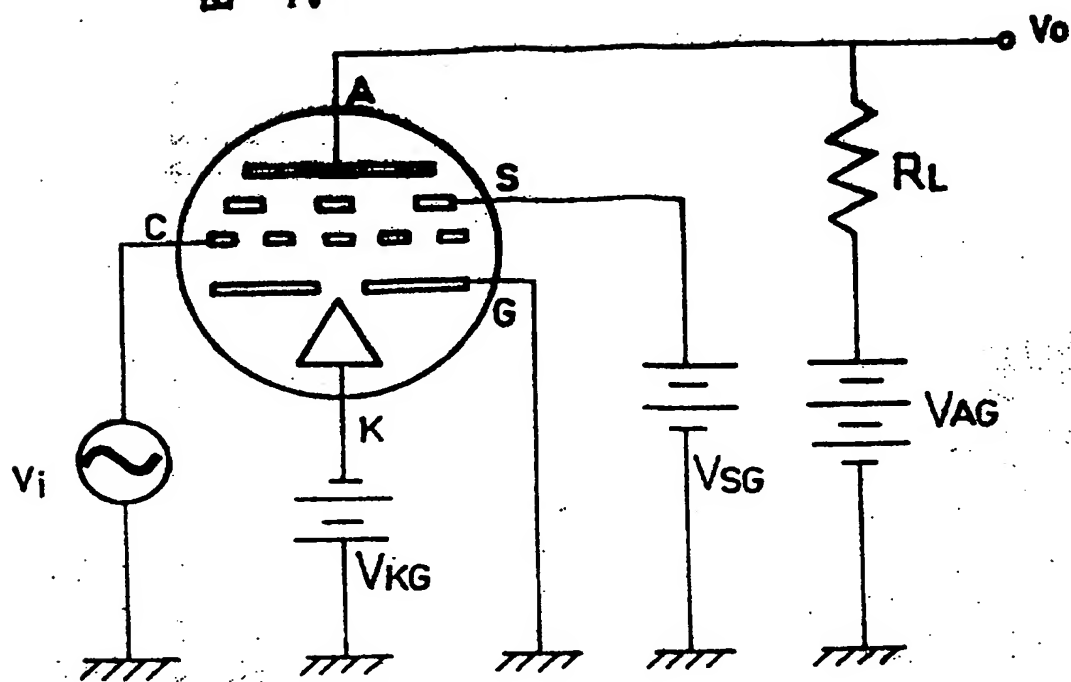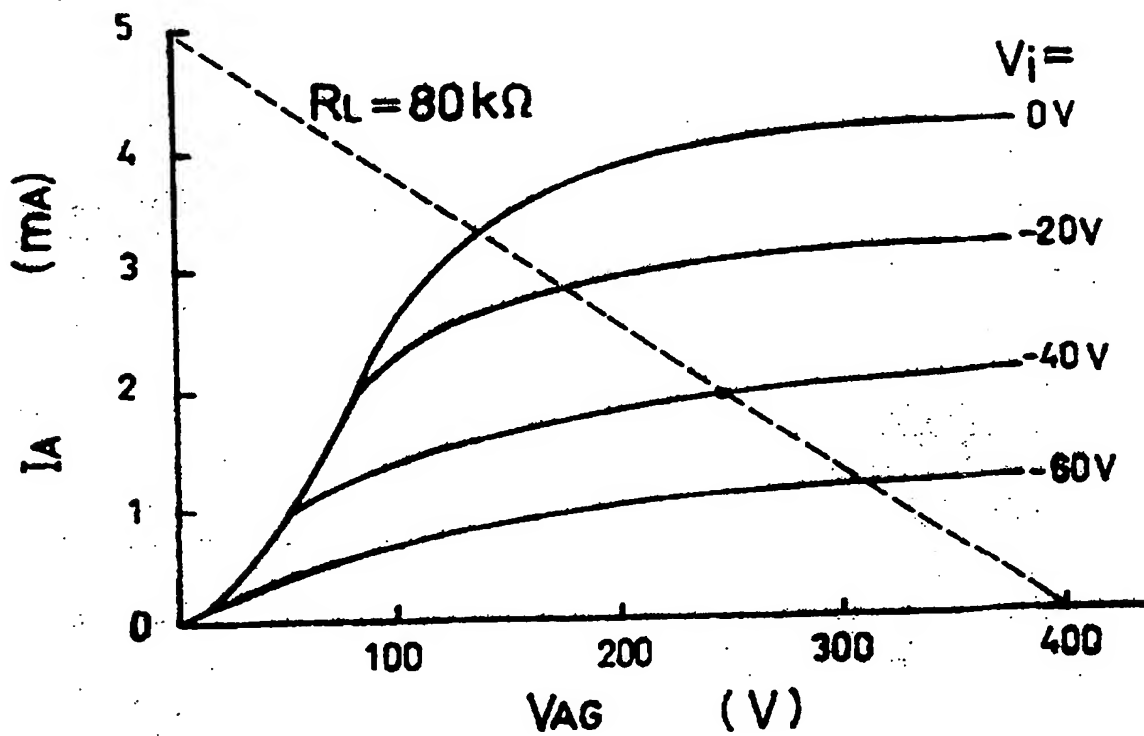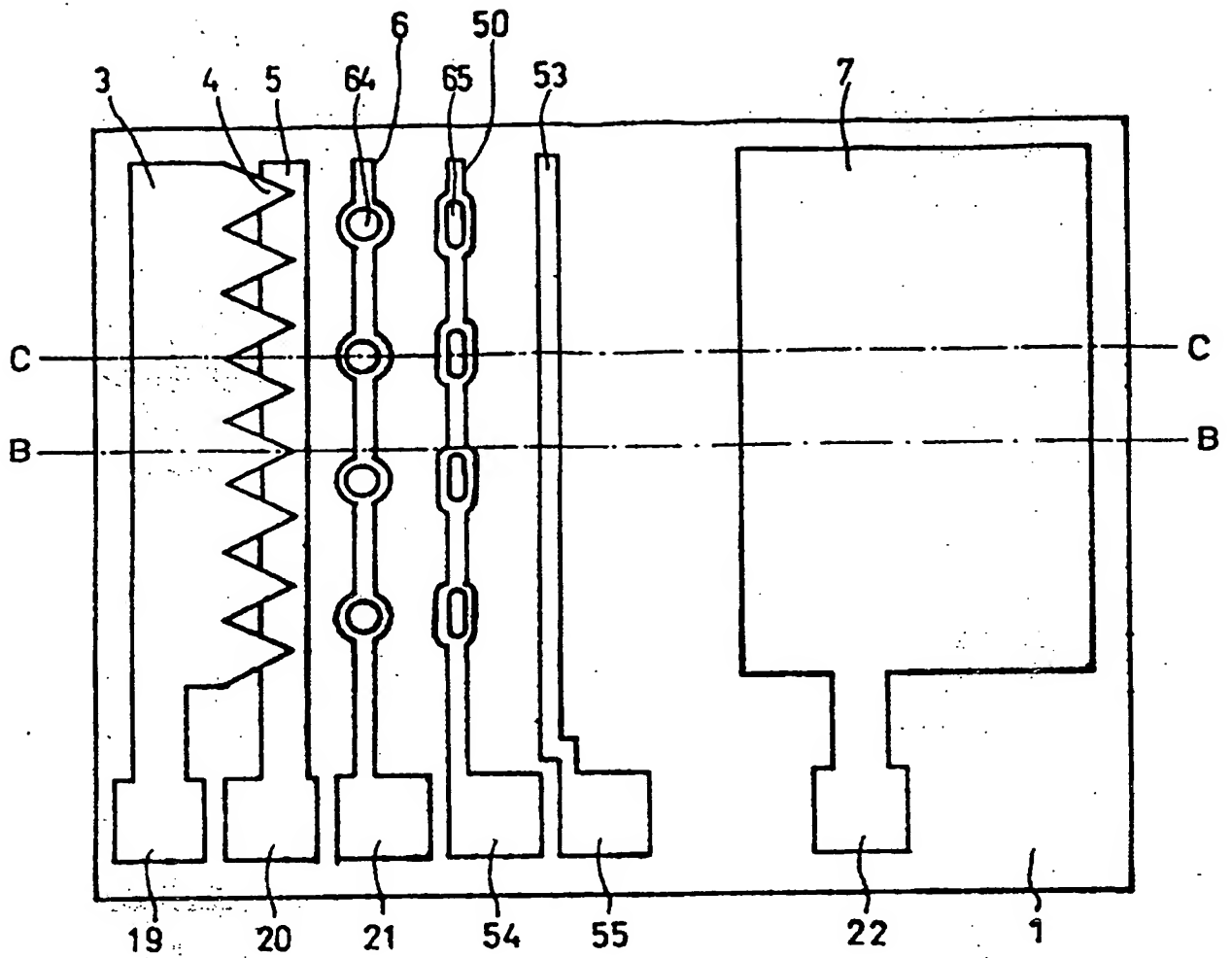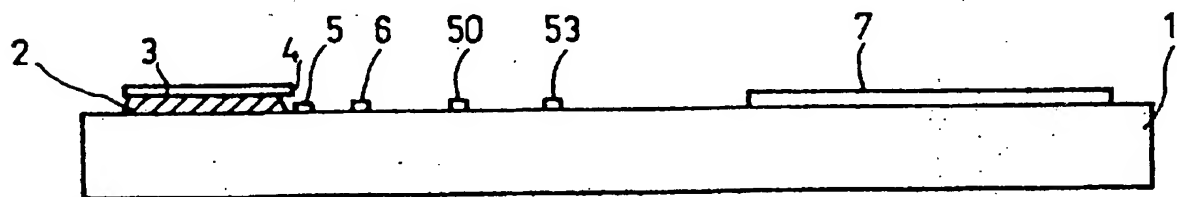
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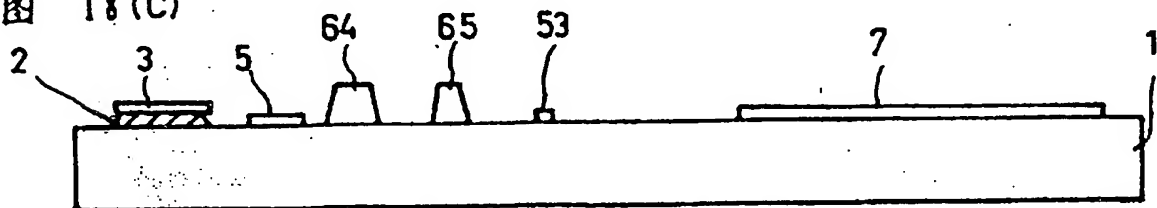
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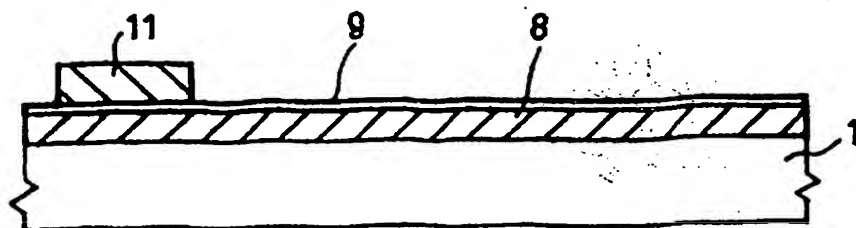
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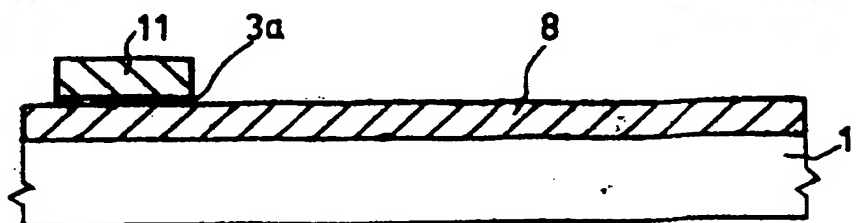
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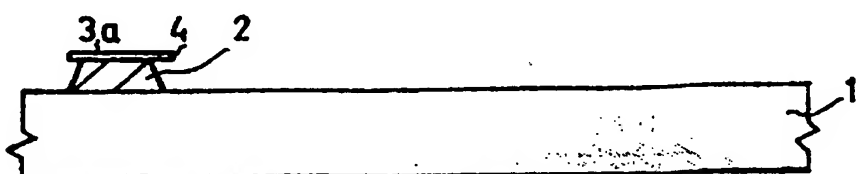
图 19(D)

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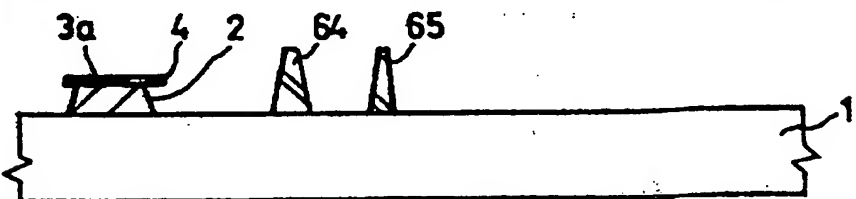
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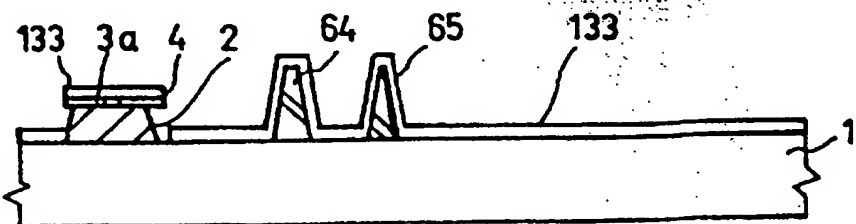
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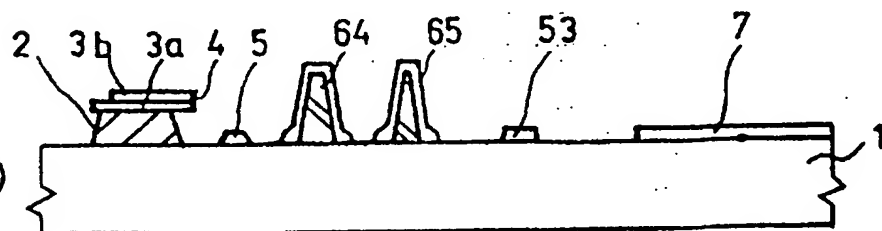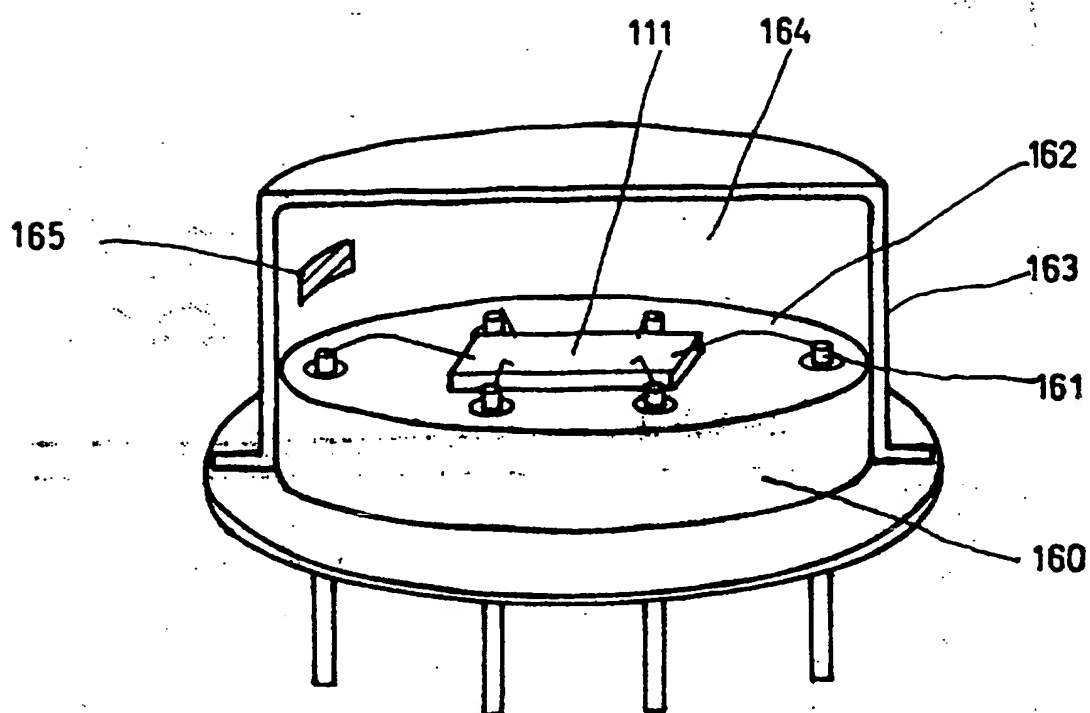
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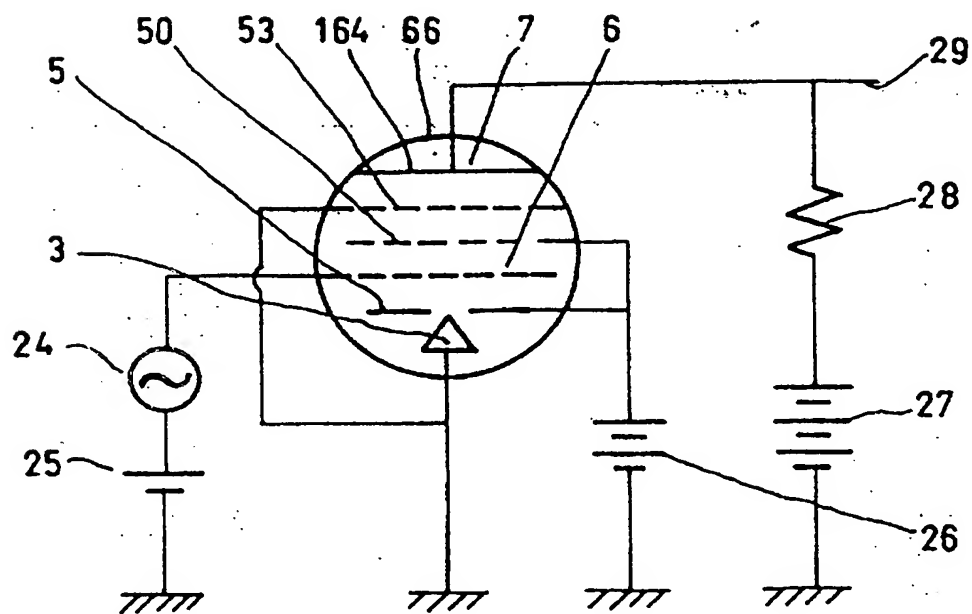
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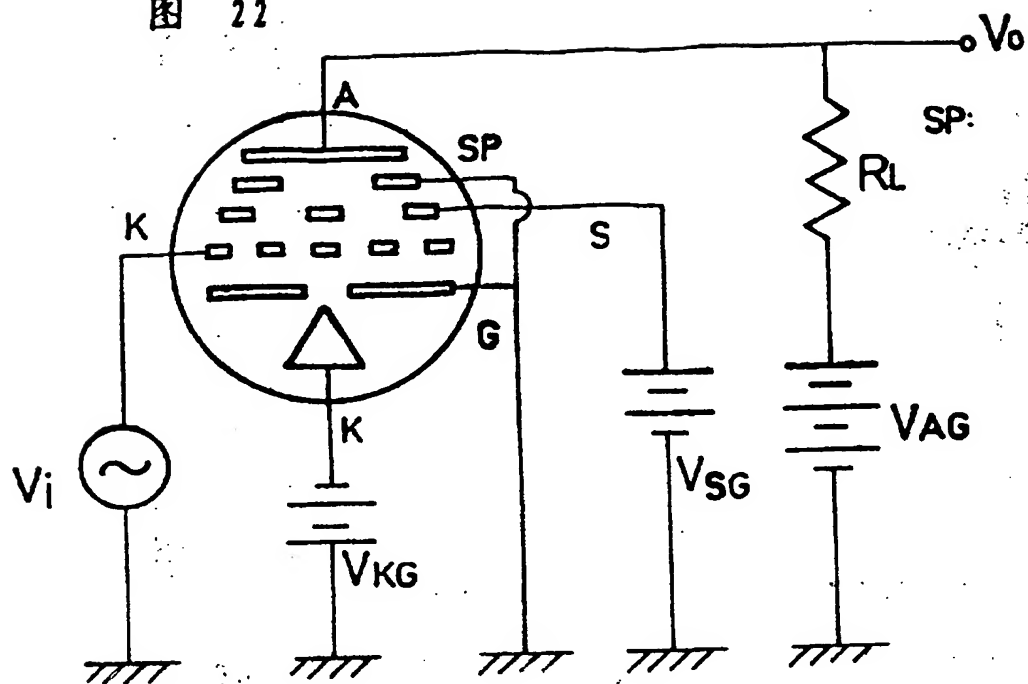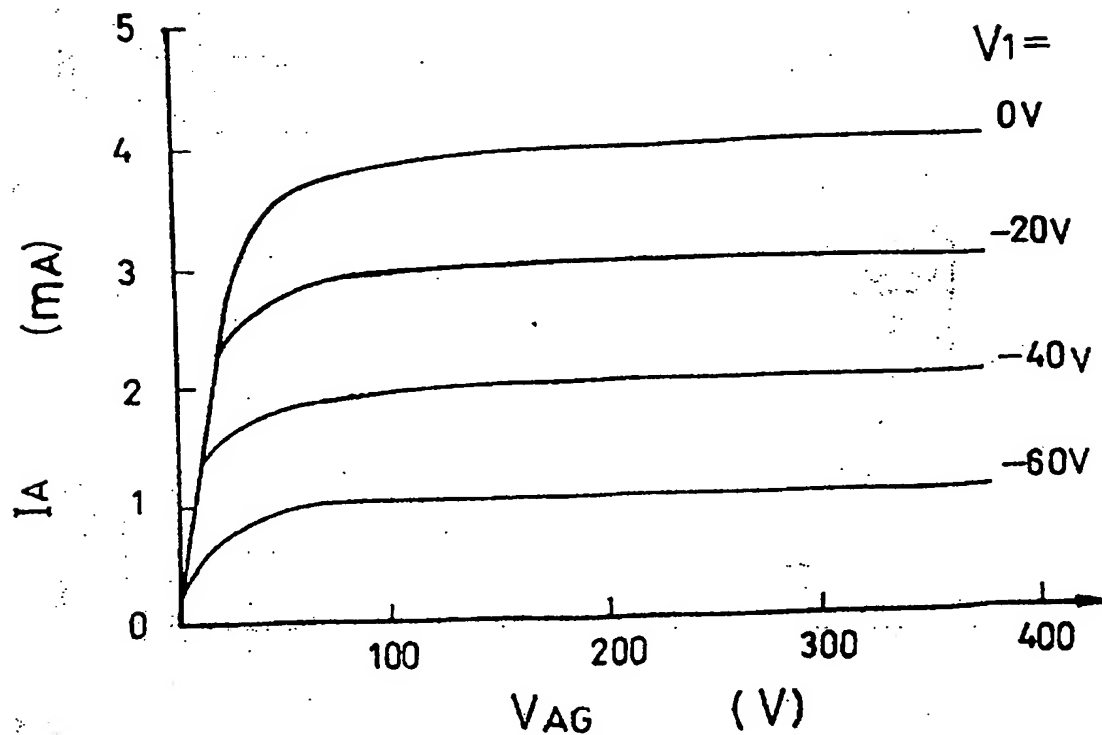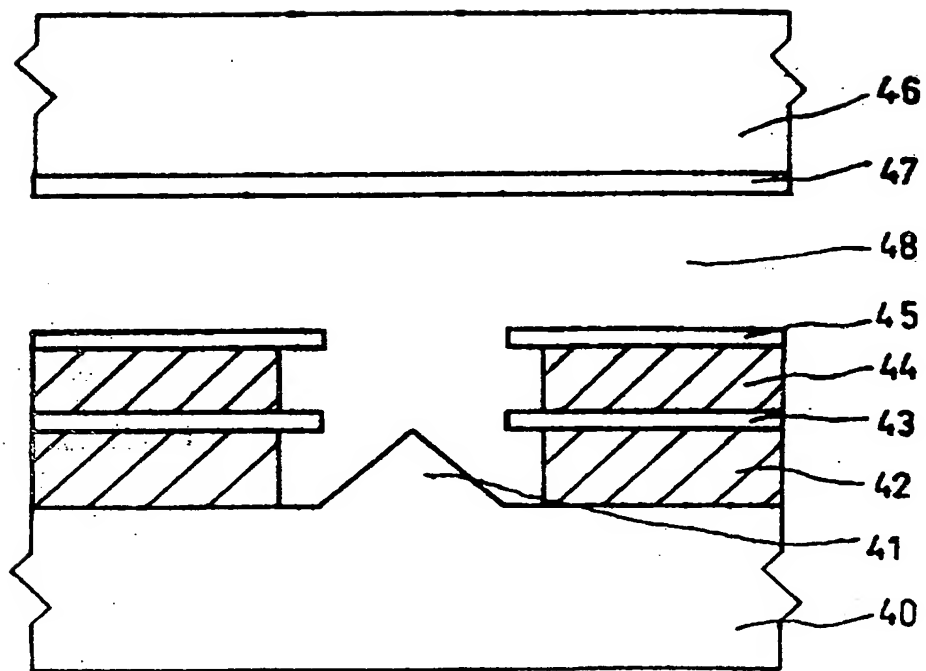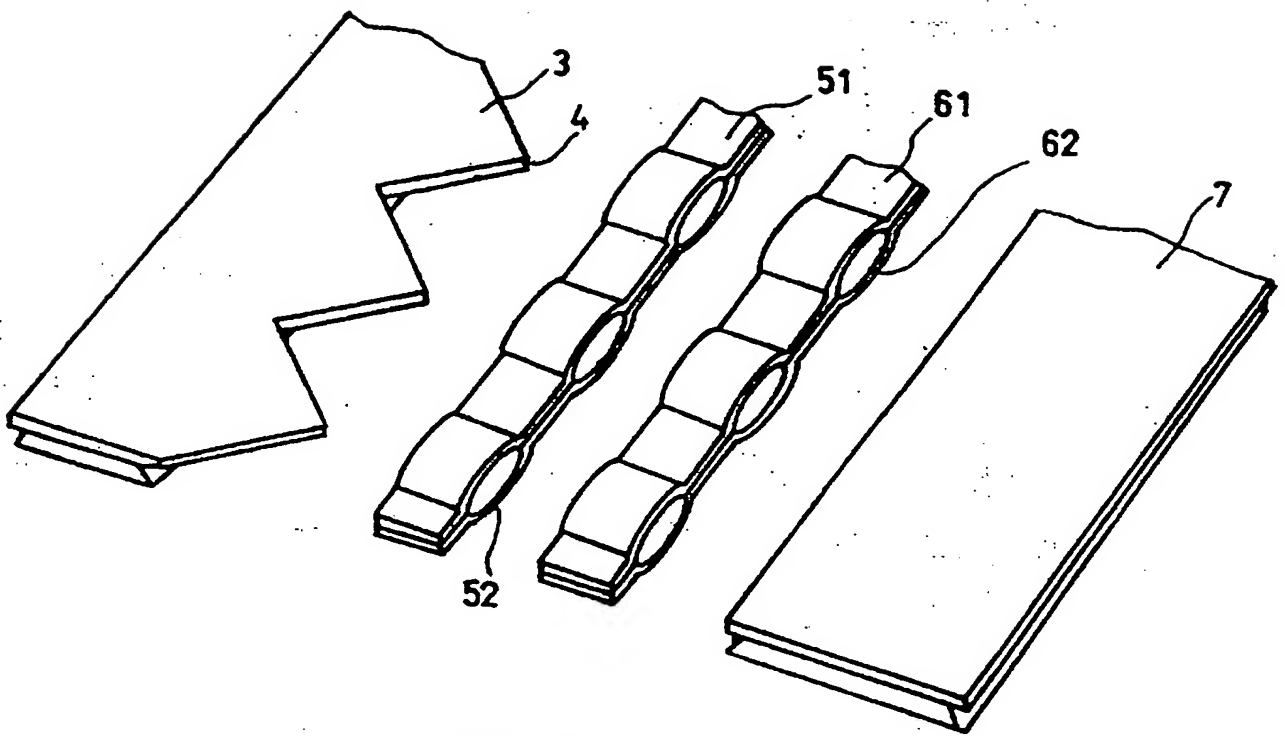
62

图 22

图 23

图　24

图 25

图 26

图 27(a)

图 27(b)

图 27(c)

图 27(d)

图 28(a)

1 311 312

图 28(b)

b

313

314

b

图 28(c)

315 314 312

311

1

图 29(a)

图 29(b)

图 29(c)

图 29(d)

69

图 30（a）

図 322

図 314

図 312

図 311

図 1

321

図 30（b）

321 312

311

図 31

323

322

314

312

311

1

321

70
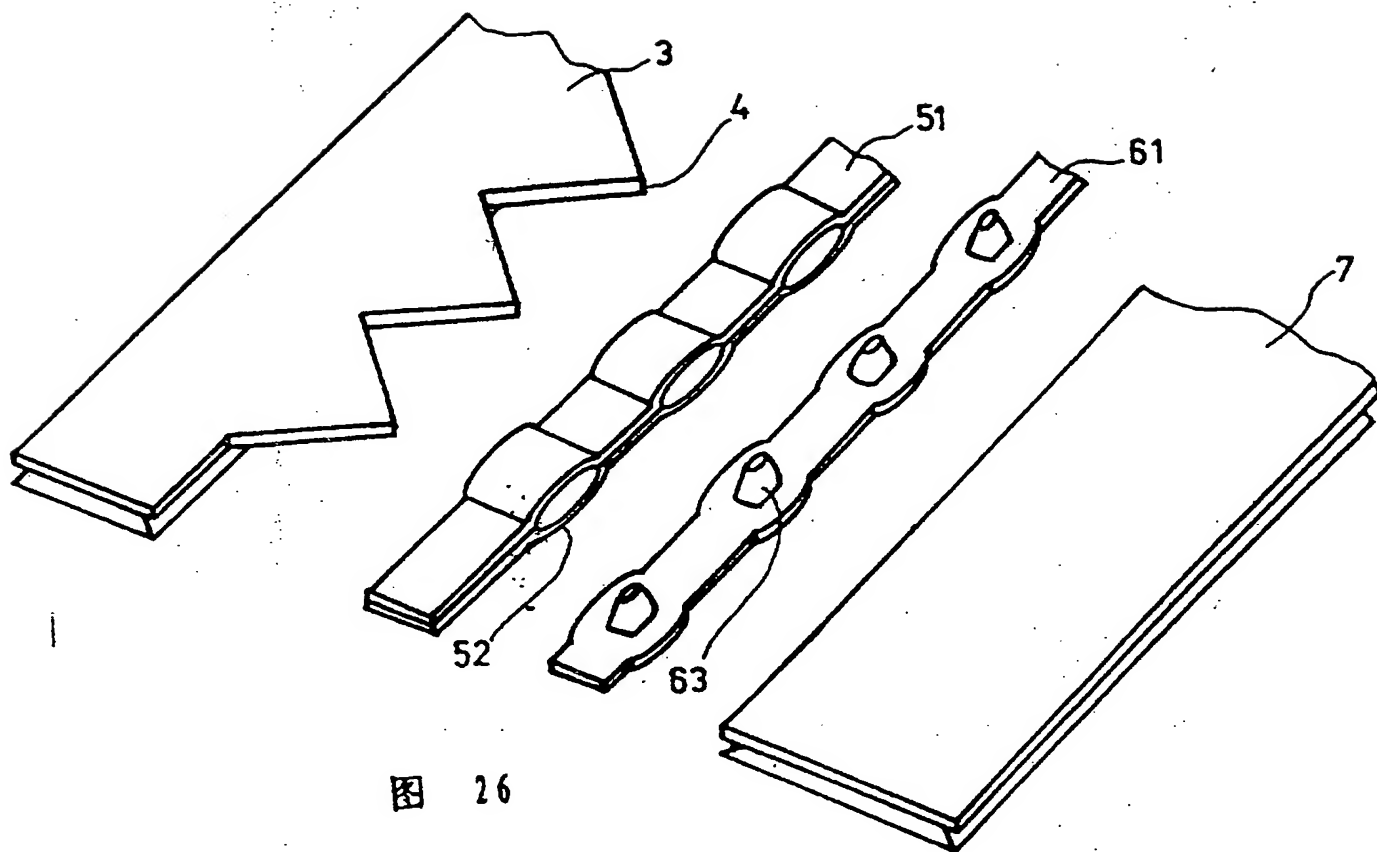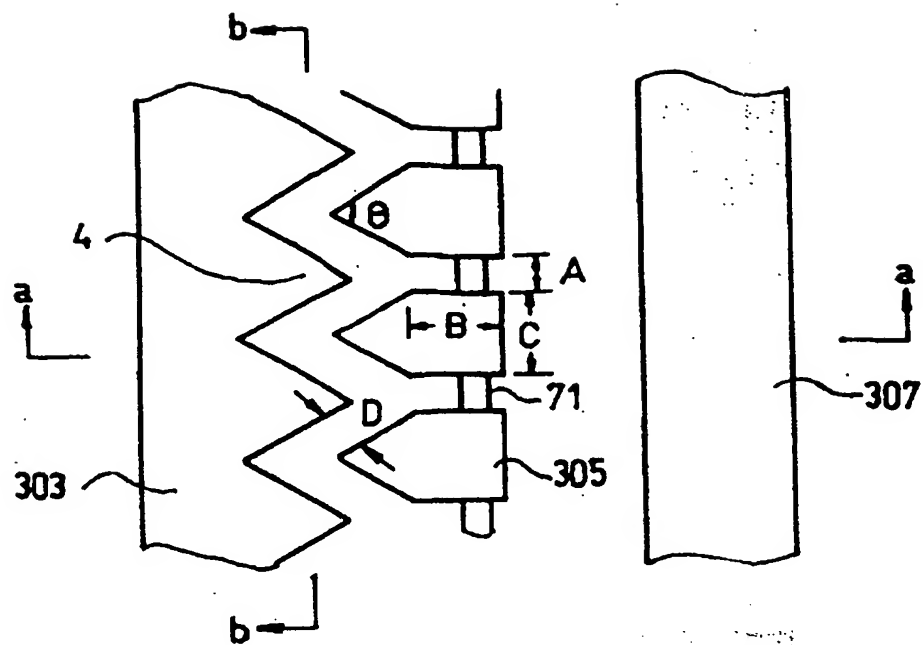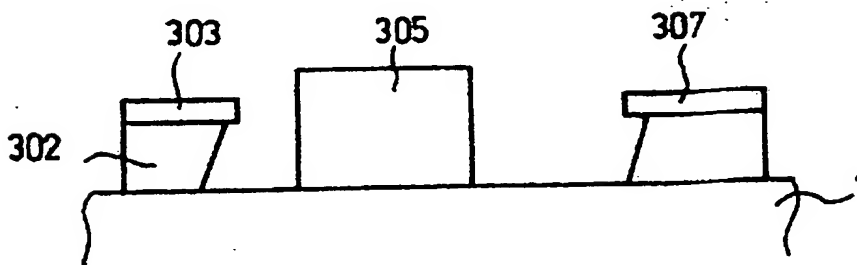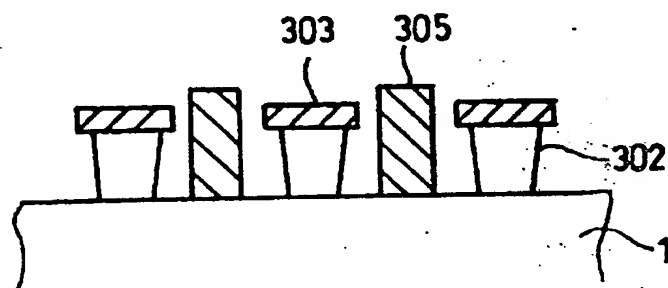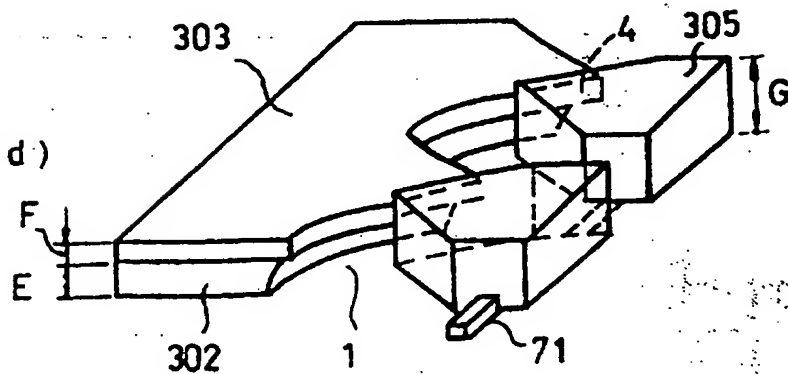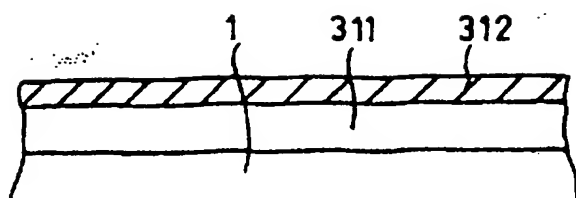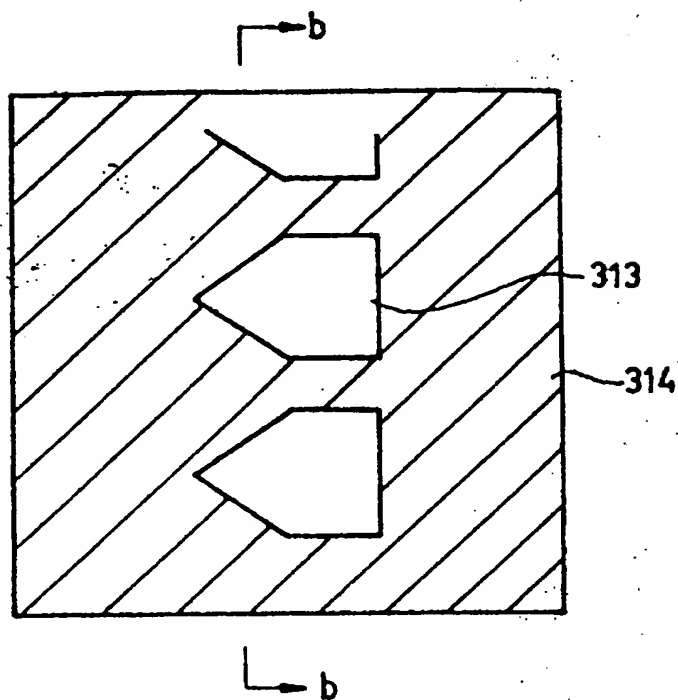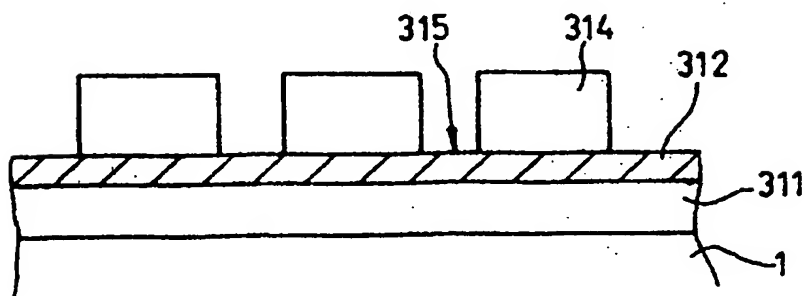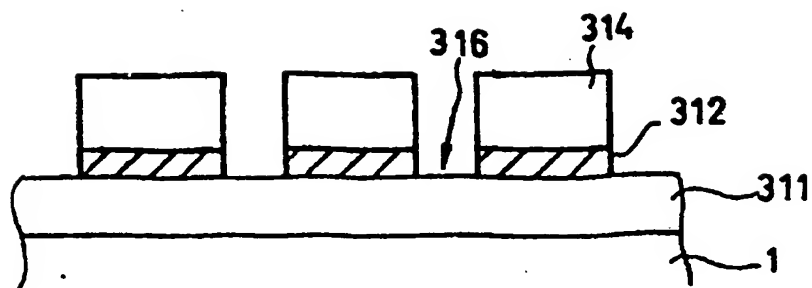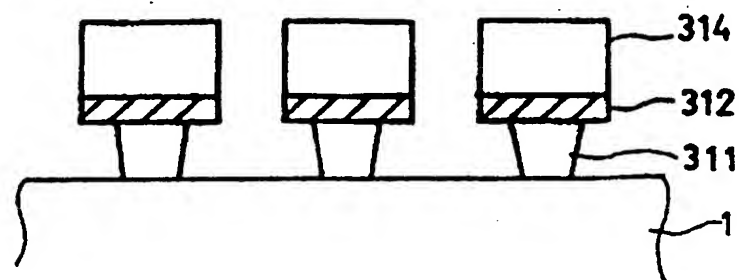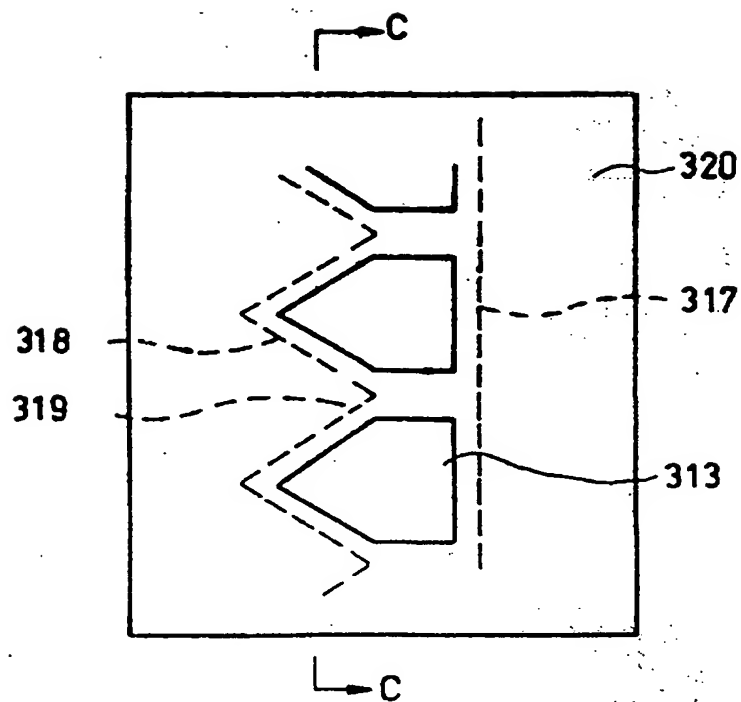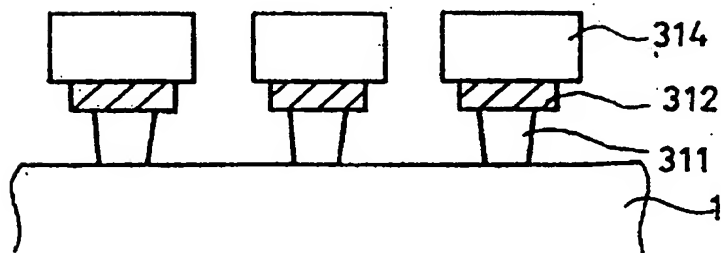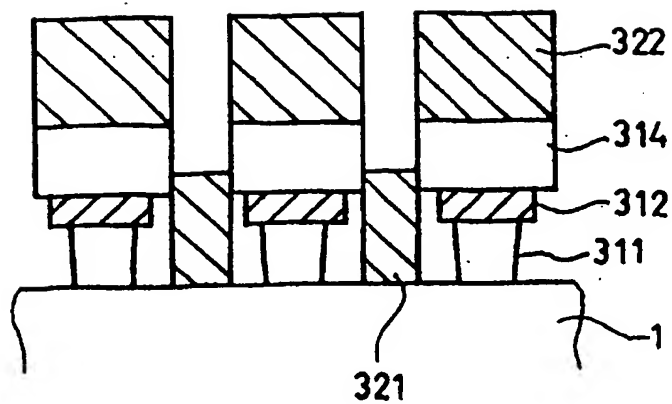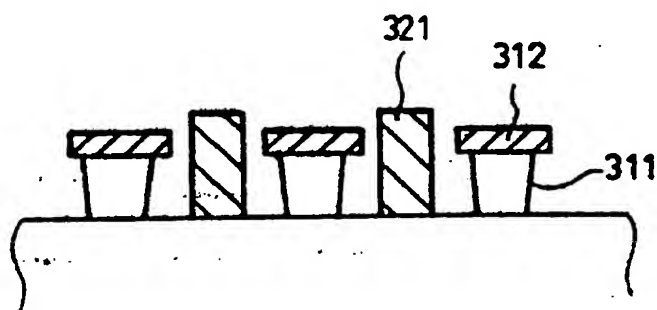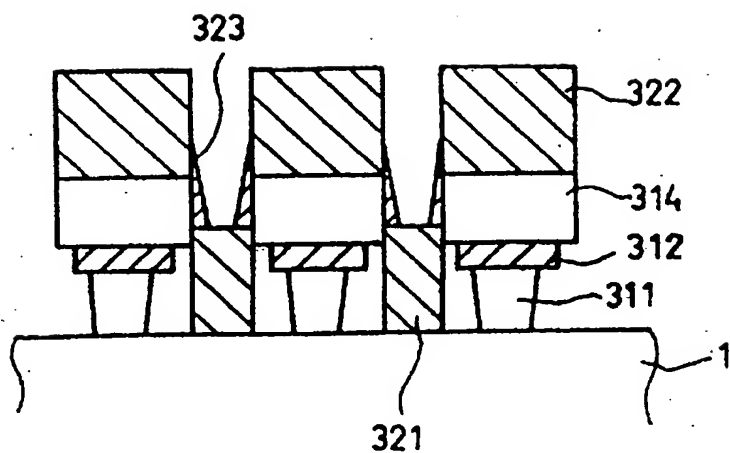
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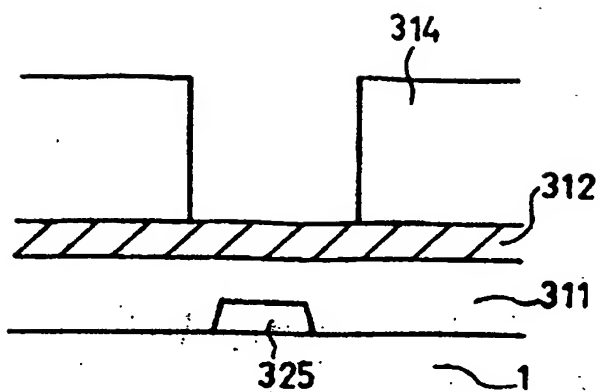
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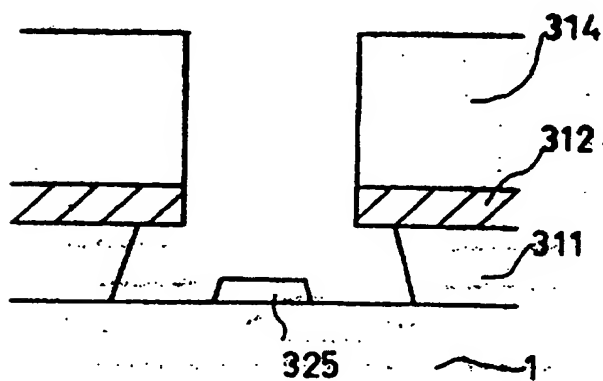
图 32（c）

图 32(d)

图 32(e)

图 32(f)

72
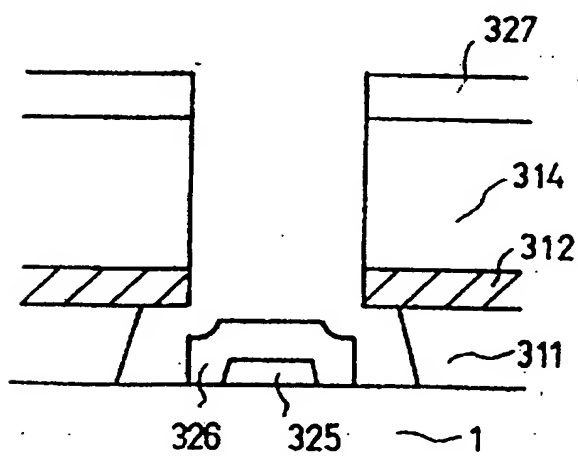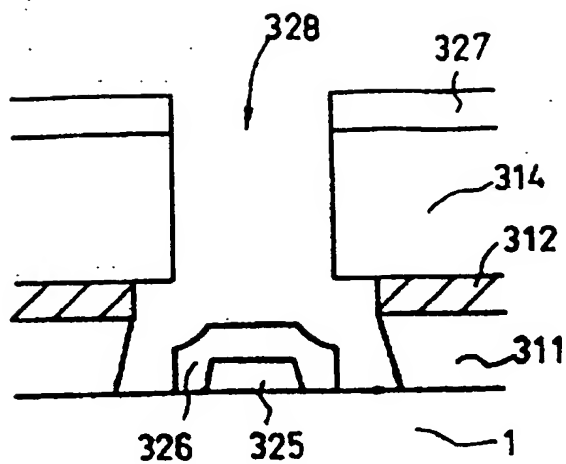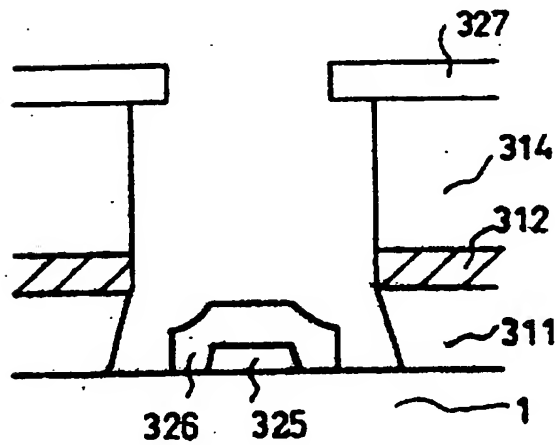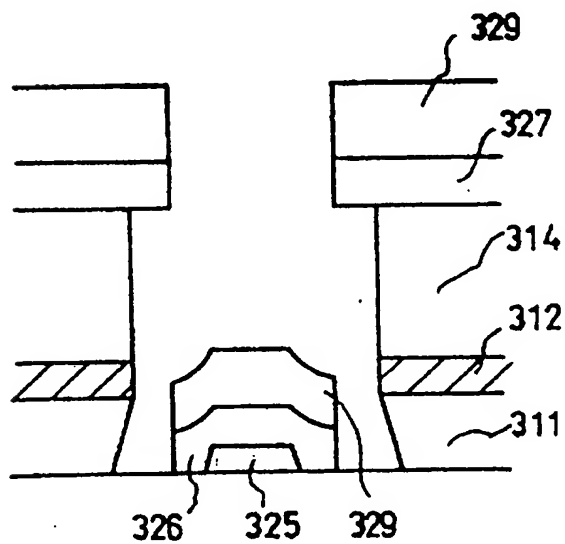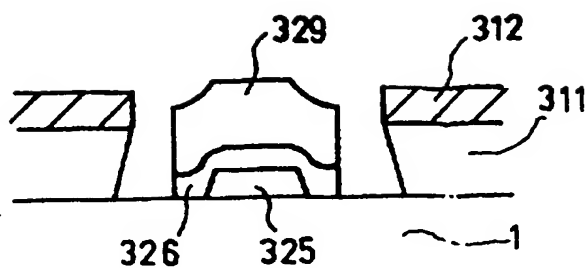
图 32(9)

图 33
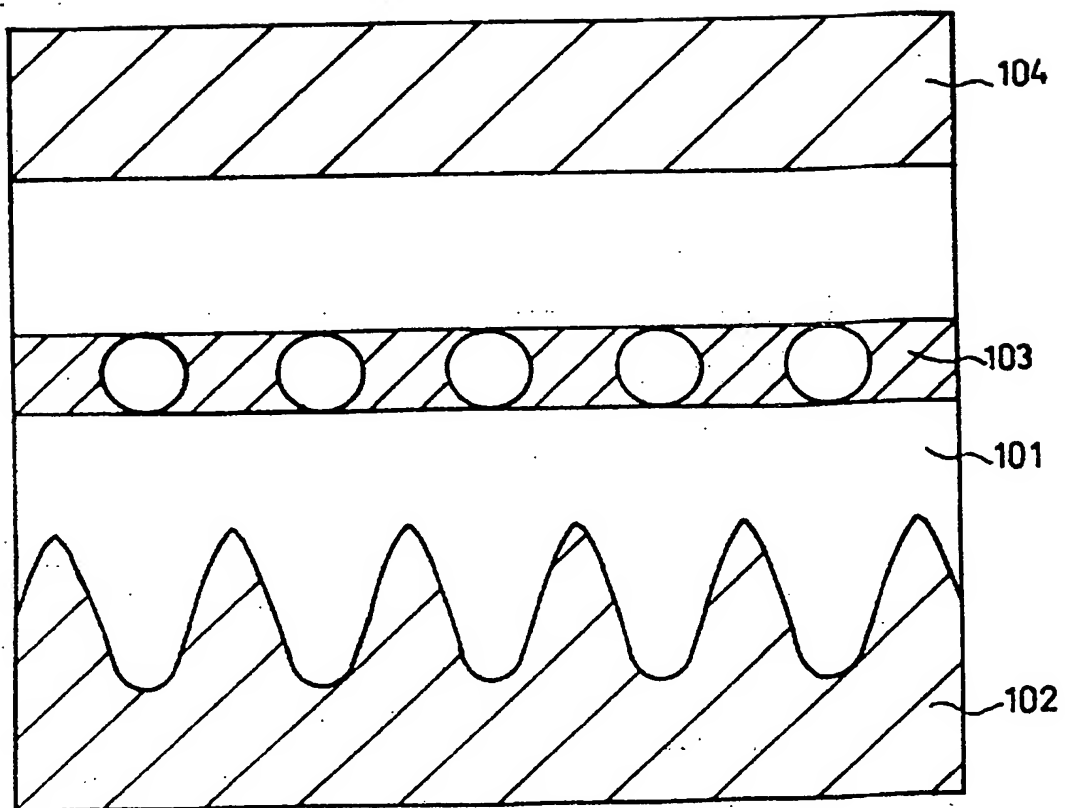
MULTIPLE ELECTRODE FIELD ELECTRON EMISSION

DEVICE AND METHOD OF MANUFACTURE

This invention relates to a multiple electrode field electron emission device which controls field-emitted electrons originating from a cold cathode. More specifically, this invention relates to a multiple electrode field electron mission device having a linearly related input signal voltage and anode current. The device is useful in applications, such as, power amplifiers, linear amplifiers, and switching circuits.

An example of a multiple electrode field electron emission device is reported by [Junji] Ito in *Journal of Applied physics,* Volume 59, number 2, pages 164 to 169 (1990). A generalized illustration of such a prior art multiple electrode field electron emission   device is shown in FIG. 33, and is referred to a flat triode device. It has such a structure in which a wedge shaped emitter electrode (cathode) 102 , a column shaped gate electrode 103, and a anode 104 are sequentially fabricated on the surface of a quartz substrate 101. The triodes are formed by using a photo-etching process to deposit and shape a thin tungsten film one micron thick. The emitter electrode 102 has a pitch of 10 microns and has 170 emission projections. The distance between gate electrode 103 and emitter electrode 102 is 15 microns. The distance between the gate electrode 103 and anode 104 is 10 microns.

When the electrical properties of this triode device are measured in a vacuum of 5×10^{-6} pa, the emission current of emitter is a Fowler-Nordheim (F.N) tunnel current. With the gate and anode voltages set at 220 V and 318 V, respectively, an anode current of about 1.2 micro-amps is obtained. This amounts to about 7 μA of anode current for each emitter electrode element and the mutual conductance for these elements is about 0.1 μs.

However, such a prior art triode device structure has a number of potential problems, which will be discussed hereafter. That is, part of electrons emitted from electrode 102 toward anode 104 flow to positively biased gate electrode 103 because of its intermediate position between the two other electrodes 102 and 104. Because the gate currents equal to or higher than the anode current, the gate input resistance is very small. That is, the electron

yield (anode current divided by total emission current) flowing to anode 104 decreases, causing a reduction in electrical properties because characteristics such power efficiency and mutual conductance are reduced. Therefore, this technology provides about a 60% yield. When controlling anode current of triode device with a low input resistance triode, in order to apply inputting signal to gate electrode 103, it is necessary to provide a drive circuit which can control parameters such as large current and large power and so on. This limitation makes it difficult to use the prior art triode devices as current amplifiers and power switches.

In addition, the triode emission current of emitter electrode is in the form of Fowler-Nordheim (F-N) tunnel current which increases or decreases exponentially relative to changes in the gate voltage. As a result, the anode current changes exponentially along with the gate input signal. Triode devices possessing this type of non-linear input and output relationship, are not capable of being used for applications such linear amplifiers.

Furthermore, in order to increase performance by enlarging the mutual conductance of the triode device, it is necessary to modified the gate electrode 103 structure and enlarge the emission surface area of emitter electrode 102. However, enlarging the emission surface area also increases the number of electrons flowing to gate electrode 103. Therefore, a power amplifier with high performance cannot be obtained using current technology.

Cathode 102 and gate electrode 103 are typically fabricated during the same photo-etching process. Electrode separation is determined by the resolution of the photoresist when which is exposed, and is practically limited to 0.8 microns. Furthermore, as process geometries become smaller, variations increase. The magnitude and uniformity of the threshold voltage for electron emission in the field electron emission device largely depends on the distance between cathode 102 and gate electrode 103. As a result reducing threshold voltage in current triode devices is difficult and even when successful provides poor uniformity.

The threshold voltage of the field electron emission device also depends chiefly on the radius of curvature for the tip of the cathode 102 elements. That is, the smaller the radius of curvature for an electrode tip, the lower the threshold voltage. To obtain a practical

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threshold voltage, it is desirable to have a tip radius of curvature of 1000 angstroms or less. However, fabrication of a practical tip radius of curvature is difficult with current processing technology, which is generally limited to 2000 angstroms because of photoresist seepage.

Therefore, the present invention was developed to overcome these problems found in the art. Purposes and objectives of the invention include offering a high performance multiple electrode field electron emission device with a large gate input resistance, a linear input and output relationship and a large mutual conductance, and offering a manufacturing process for such a multiple electrode field electron emission device.

The multiple electrode field electron emission device of the invention is characterized by comprising at least one field effect electron emitting cathode, a gate electrode for applying an electric field to the cathode, an anode collecting the emission electrons, and a control electrode disposed between the cathode and the anode so as to control the aforesaid electron emission. Another features of the invention is, comprising at least one island shaped insulating layer, which is formed on one surface of a insulating flat substrate; a cathode, which has one or more emission projections that overhang the edge of the island shaped insulating layer; a gate electrode, which is formed on the aforesaid flat substrate surface in a generally vertical proximity to the emission projections; an anode, which is formed on the aforesaid flat substrate surface, and a control electrode is disposed on the aforesaid flat substrate and between the aforesaid gate electrode and the aforesaid anode.

Moreover, the multiple electrode field electron emission device of the invention is characterized by a screen electrode which is formed between the aforesaid control electrode and the aforesaid anode to electrostatically screen the aforesaid control electrode and the aforesaid anode; and a suppresser electrode which is disposed between the aforesaid screen electrode and the aforesaid anode to control secondary electron emitted by the anode.

The method of manufacturing the field electron emission device of this invention comprises the processes of forming a cathode possessing one emission projection projected substantially parallel to the surface of the flat substrate, the process including at least depositing and forming an etching mask layer on the aforesaid flat substrate, depositing and

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forming a cathode on the surface of the aforesaid etching mask layer, depositing and forming an etching passivation layer on the surface of the aforesaid cathode; the process of processing the aforesaid etching mask layer to form an etching mask for the emission projection; and the process of forming the cathode layer in the shape of the aforesaid etching mask so to create a cathode with emission projections.

In addition, the method of manufacturing the field electron emission device of this invention comprises at least the processes of forming an etching mask layer on the surface of a flat substrate; forming a cathode layer on the surface of the aforesaid etching mask layer; forming a resist layer on the surface of the aforesaid cathode layer; processing the cathode layer in the shape of the surface of the aforesaid resist layer; processing the aforesaid etching mask layer using an over-etching method to form an etching mask; removing the aforesaid etching mask from a lower periphery of the cathode and patterning the cathode in the shape of an cave; forming a gate electrode layer using directional particulate deposition; and processing the aforesaid gate electrode layer to form a gate electrode.

The multiple electrode field electron emission device of the invention comprises a cathode forming on an insulating layer formed on a surface of a insulating flat substrate, the cathode having a plurality of projections projected from the insulating layer; an anode formed on a surface of the said flat substrate and collecting emitted electrons; a gate electrode which is formed between the said cathode and the said anode and has an opening at a position of the projection; and a control electrode formed between the said gate electrode and said the anode.

The multiple electrode field electron emission device of this invention comprises at least a cathode that emits electrons according to field effect; a gate electrode that applies an electric field on the aforesaid cathode; an anode that collects emitted electrons; and a control electrode that is placed between the aforesaid cathode and the aforesaid anode to control the aforesaid emitted electrons. In addition to the aforesaid cathode, the gate electrode, the control electrode, and the anode, it further comprises another control electrode formed between the aforesaid control electrode and the aforesaid anode; an screen electrode which electrostatically screens the electrostatically anode; and a suppresser electrode formed

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between the aforesaid screen electrode and the aforesaid anode to control the secondary electrons of the aforesaid anode.

The cathode of the invention is formed on the surface of the insulating layer that is formed on the insulated flat substrate, and has emission projections that overhang from the insulating layer. The insulating layer may be formed in the shape of an island in correspondence with the shape of the emission projections. The opening in the gate electrode layer is for the purpose of efficiently collecting emitted electrons from the cathode on the anode. If, for example, the opening was a ring shape and was formed at the corresponding position of the projection, there would be a remarkable reduction in the volume of electrons that flow to the gate electrode and the gate input resistance would become very high. That is the gate and control currents decrease as result of emission current flowing trough the inside of the opening of the ring shape and parasitic currents also decrease.

Embodiments of the invention are described hereafter. FIG. 1 is a cross sectional schematic view of a part of a tetrode field electron emission device. In FIG. 1, a gate electrode 5 and control electrode 6 in the device are formed of molybdenum thin film of 1000 angstroms, and disposed on a surface of a flat substrate 1. An insulating layer 2, which is of 5,000 angstroms thick and made of silicon dioxide and adjacent to both gate electrode 5 and control electrode 6. A cathode 3 is formed on one surface of insulating layer 2 adjacent to gate electrode 5, and is 2,000 angstroms thick. The cathode 3 is configured with overhanging emission projections 4. An anode 7 is formed on the surface of insulating layer 2 adjacent to control electrode 6, which is 2,000 angstroms thick.

Cathode 3 is formed as following: a first deposited cathode fryer (3a) is tungsten (W) film with a thickness of 1,000 angstroms and a second deposited cathode layer (3b) is molybdenum (Mo) film with a thickness of 1,000 angstroms. Like cathode 3, the structure of anode 7 is such that a first anode layer (7a) and a second anode layer (7b) are both deposited. The tetrode, that is, cathode 3, gate electrode 5, control electrode 6 and anode 7, are placed on the surface of flat substrate 1 in this respective sequence.

Cathode 3 is configured to have multiple emission projections 4 which are aligned in a row with a pitch of 5 microns. Emission projections 4 are structured so that they project parallel to the direction of gate electrode 5 which is on the surface of flat substrate 1. Island shaped insulating layer 2 is patterned so that it does not exist in the vicinity of the emission projection tips. The radius of curvature for the tip of emission projections 4 along the flat direction is about 400 angstrom.

Gate electrode 5 is formed so that it self-aligns to cathode 3 and has a recession area of nearly the same shape as the emission projections 4 in the lower vertical portion of emission projections 4. The distance (Lgk) between gate electrode 5 and emission projections 4 is determined by the film thickness of island shaped insulating layer 2 and gate electrode layer 5. This is a value for which the film thickness of gate electrode S is subtracted from the film thickness of island shaped insulating layer 2 (Lgk=4,000 angstroms). Based on recent methods of structuring thin films, the control of the film thickness is very good. As a result the controllability of Lgk and reproducibility and uniformity of this device are excellent

The width of gate electrode 5 in the vicinity of tips of the emission projection 4 is about 2 microns. The distance (spacing) between gate electrode 5 and control electrode 6 is 4 microns. The width of control electrode 6 is 8 microns. The distance (spacing) between control electrode 6 and anode 7 is 10 microns. The smaller the width of gate electrode 5, the smaller the gate current and the better the power efficiency. Also, the larger the width and surface area of anode 7, the higher the electron yields. The wider control electrode is, the larger the mutual conductance and the greater the controllability of the anode current. However, because the width quantity of electrons (control current) that flow to control electrode 6 increases, the width of the control electrode is determined by a balance between these parameters. It is ideal to have dimensions in a range in which the width of control electrode 6 is greater than the width of gate electrode 5 but smaller than the width of anode 7. To increase the amplification factor ($\mu=C_{CG}/C_{AG}$,where C_{CG} is the capacitance between gate electrode 5 and control electrode 6, and C_{AG} is the capacitance between gate electrode 5 and anode 7.), means decreasing the width of control electrode 6 and enlarging the space between control electrode 6 and anode 7.

FIG. 2 illustrates the process of manufacturing the tetrode field electron mission device shown in FIG. 1. It is a longitudinal cross sectional view in a state in which the main structural manufacturing processes have been completed. FIG. 2(A) shows the device after sequential formation of insulating layer 8, cathode 9, and etching passivation layer 10 on the surface of flat substrate 1 and after formation of photoresist layer 11. Flat substrate 1 is an insulating quartz material. Insulating layer 8, cathode 9, and etching passivation layer 10 are deposited in turn using a sputter deposition process. Insulating layer 8, cathode 9, and etching passivation 65 layer 10 are composed of a 5,000 angstrom silicon dioxide thin film, a 1,000 angstrom tungsten thin film and a 2,000 angstrom silicon dioxide thin film, respectively. Photoresist layer 11 is patterned after a desired shape for cathode 3 and anode 7.

FIG. 2(B) is a cross sectional view of the device after fabrication of the etching mask by etching passivation layer 10 through over-etching. The over-etching technique employs HF(hydrofluoric acid) type etching solution which selectively etches passivation layer 10 so that etching passivation layer 10 etched away is more than what is delimited by the shape of photoresist layer 11. It is possible to obtain etching mask 12, which has small radius of curvature emission projections 4, by etching passivation layer 10 more than the curvature radius of the area on photoresist layer 11 that corresponds to emission projection 4, front the outer periphery inward. In this embodiment, the curvature radius of photoresist layer 11 is 3.000 angstroms. Therefore, about 5,000 angstroms of over-etching are used to obtain etching mask 12, which has a tip curvature radius of 300 angstroms.

FIG. 2(C) is a cross-sectional view of the device after cathode layer 9 has been fabricated and after the first cathode layer (3a) and the first anode layer (7a) have been formed. Etching mask 12, which will have sharp emission projections after the removal of photoresist layer 11, is used to fabricate cathode layer 9. Dry etching is used to fabricate cathode layer 9. Dry etching takes place for five minutes at a gas flow ratio of CF_4/O_2=60/120 and a radio power of 700 watts. At this time, cathode 9 is over-etched to obtain the first cathode layer (3a), which exhibits sharp emission projections with a tip curvature radius of 300 angstrom.

FIG. 2(D) is a cross-sectional view of the device after the insulating layers has been etched away in sections, forming island shaped insulating layer 2, and exposing emission projections 4. First cathode layer (3a) and first anode layer (7a) are used as etching masks to remove the unnecessary portion of insulating layer 8 with an HF etching solution and form island shaped insulating layer 2. At this time, emission projections 4 are exposed such that they overhang from island shaped insulating layer 2. Also, etching mask is removed and flat substrate 1 shows almost no etching because it is made of quartz.

FIG. 2(E) is a cross-sectional view of the device after gate electrode layer 13 has been formed using the directional particulate deposition method. Sputtering is used as the directional particulate deposition method to deposit a molybdenum (Mo) thin film layer of 1,000 angstroms in thickness to form gate electrode layer 13. The directional particulate deposition method shoots out particles and deposits them on the surface of flat substrate 1 in a nearly perpendicular direction from the particle source. When this method is used, the overhanging portions, such as emission projections 4, become a cover, allowing molybdenum thin film layer 131, which is deposited on the top of first cathode layer (3a), molybdenum thin film layer 132, which is deposited on the surface of first anode layer (7a), and gate electrode layer 13, which it deposited on the surface of flat substrate 1, all to be electrically isolated. In addition, emission projections 4 and the overhanging portion, which has the same shape as these projections, are fabricated so that they self-align to the lower vertical portion of emission projections 4. (Even if the position of one of the electrodes is not aligned, the other electrode will be fabricated so that its position corresponds to that vertically aligned position.) Vapor deposition, sputtering, electron cyclotron resonance (ECR), plasma deposition and the clustered ion beam can be used as the directional particulate deposition method.

FIG. 2(F) is a cross-sectional view showing the device after gate electrode 13 and molybdenum thin film layers 131 and 132 have been etched and after second cathode layer (3b), gate electrode 5, control electrode 6, and second anode layer (7b) have been fabricated. After photo-etching technology is used and the overhanging portions of emission projections 4 and gate electrode 5 have been covered with photoresist, the molybdenum thin film is

etched by employing dry etching.

The tip curvature radius of emission projections 4 of the cathode 3 of a completed multiple electrode field electron emission device is 400 angstroms. This is due to first cathode layer (3a) having more roundness because of the deposition of second cathode layer (3b). However, this roundness causes the surface area of emission projections 4 that is in the electric field to enlarge, making it possible to obtain electron emissions that are large in volume and are stable. Where the materials used for first cathode layer (3a) and second cathode layer (3b) are different, for the most part, if either the emission projections part of first cathode layer (3a) or second cathode layer (3b) are etched away, emission projections 4 will become thinner and the film thickness direction tip curvature radius becomes smaller, making possible a multiple electrode field electron emission device that has a low threshold value.

If the distance between the cathode and the gate electrode are uniformly shortened and the radius of curvature for the emission projection tips are made small, the threshold voltage is reduced. The manufacturing process for this configuration is described using a triode field electron emission device.

FIG. 3 is a perspective view of a triode field electron emission device manufactured employing this manufacturing process and procedure. The major components of the device are flat substrate 1; island shaped insulating layer 202; cathode 203, which is equipped with emission projections 4 which are formed as overhangs on the surface of the cathode; gate electrode 205, which is formed so that it self-aligns to emission projections 4; and anode 7, which is formed on the surface of flat substrate 1. Around island shaped insulating layer 202, particularly in the vicinity of gate electrode 205 on flat substrate 1 is slope 213. Slope 213 has the advantage of reducing the situations in which electrons emitted from emission projections 4 flow to gate electrode 205, and it improves the power efficiency of the field electron emission device.

The field electron emission device has 100 emission projections which have 5 micron pitch and are aligned in a row. The tip curvature radius of emission projections 400 angstroms. The distance (L_{GK}) between cathode 203 and gate electrode 205 is 4,000

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angstrom. The width of gate electrode 205 at the tip of the mission projection (4) is 2 microns. The distance (L_{GK}) between cathode 203and anode 7 is about 10 microns. Flat substrate 1 may be made of a 7059 glass substrate manufactured by Coning Corporation. Island shaped insulating layer 202 is made of a 5,000 angstrom thick silicon oxide film, and first cathode (203a) is made of a 1,000 angstrom thick molybdenum (Mo) thin film. Second cathode (203b), gate electrode 205, and anode 7 are all made of a 2,000 angstrom thick tantalum (Ta) thin film. The angle of slope 213 is approximately 10 degrees.

FIGS. 4(A)-4(F) are cross-sectional views of flat substrate 1 at the completion of the main manufacturing steps for the field electron emission device shown in FIG. 3. FIGS. 5(A)-5(C) are illustrations of flat substrate 1 that correspond to FIGS. 4(B), 4(D), and 4(E), respectively. The manufacturing process of the field electron emission device of this embodiment will now be described.

First, insulating layer 8 and cathode layer 9 are formed on the surface of flat substrate 1 followed by resist layer 11 as illustrated in FIG. 4A. Flat substrate 1 is manufactured from material such as #7059 glass which has insulating properties. Insulating layer 8 is a 5,000 angstrom thick, thin silicon dioxide film layer formed using atmospheric pressure CVD techniques. Cathode layer 9 is a 1,000 angstrom thick thin molybdenum (Mo) film layer deposited using sputtering. Photoresist layer 11 is generally in the shape of cathode 203 and is formed using photo-etching.

Next, cathode layer 9 is processed according to the shaping of resist layer 11 to form temporary cathode layer 91, which is illustrated in both FIG. 4(B) and FIG. 5(A). The molybdenum thin film cathode layer 9 is etched by means of employing a dry etching method using CF_4 gas. The tip of the photoresist 11a has a tip curvature radius of 7000 angstroms, which is the same as that for temporary cathode 91.

Next etching mask layer 81 is formed by over-etching insulating layer 8. As illustrated in FIG. 4C. Over-etching is the method in which insulating layer 8 is etched away deep within a stipulated region in temporary cathode 91 using an isotropic etching meant. Because etching of temporary cathode 91 progresses at an equal rate from the outer periphery in an inward direction using the isotropic etching means, the convex areas have a

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sharp shape. As a result, there is a characteristic in which Over-etching allows a small tip curvature radius in the convex areas.

An HP type etching solution is employed as the isotropic etching means to over-etch the silicon dioxide thin film of insulation layer 8. When the outer periphery of temporary cathode 91 is etched to 1.5 microns inward, reverse taper shaped etching mask 81 is formed with a protruding portion with a tip curvature radius of 300 angstroms. Compared to the 7000 angstrom tip curvature radius of temporary cathode 91, a twenty-fold increase in sharpness is achieved. In this process, the surface of flat substrate 1 is etched to form sloped surface 213 around etching mask 81. The speed of etching the insulating layer8is five times faster compared to that of flat substrate 1. As a result the grade of the sloping surface 213 that is formed at the foot of emission projection 4 is about 10 degrees.

Next, temporary cathode 91 is etched to the shape of etching mask 81 to form first cathode 203(a), illustrated in both FIG. 4(D) and FIG.5(B). With resist layer 11 covering the surface of temporary cathode 91 for protection, when etching is performed from the back side, first cathode (203a) is formed having the same flat shape of etching mask 81. The tip curvature radius of emission projections 4 of first cathode layer (203a) is about 300 angstrom.

Next, the sides of etching mask 81 are etched away to form island shaped insulating layer 202, and resist layer11 is removed, as illustrated in both FIG. 4(E) and FIG. 5(C). About 0.7 microns of the sides of etching mask 81 are removed to form cathode (203a) in the shape of an eaves and expose emission projection 4 in the shape of overhangs.

Finally, after forming the tantalum (Ta) electrode layer using directional particulate deposition, it is etched to form second cathode (203b), gate electrode 205, and anode 7, as shown in FIG.4(F). Sputtering is employed with the directional particulate deposition to form gate electrode 205, which is made of a 2000 angstrom Ta thin film. When directional particulate deposition is employed, the overhanging portions, such as emission projection 4, become a cover, so the second cathode (203b), is deposited on the surface of first cathode (203a), and the gate electrode 205 is deposited on the surface of flat substrate 1, become electrically isolated.

The overhanging portion, which has the same shape emission projections 4, is formed so that it self-aligns with emission projection4. Sputtering, vapor deposition, ECR(electron cyclotron resonance), plasma deposition and the cluster ion beam method are some of the methods that may be used as the directional particulate deposition methods. The electrode layer of the Ta thin film is processed by means of dry etching to form gate electrode 205 and anode 7. At this time, it is important to cover the layer with photoresist so that the over-hangs are not corroded. Cathode 203 is an overlapping structure of first cathode (203a) and second cathode (203b). The tip curvature radius is about 400 angstroms. In a case in which the material used for first cathode layer (203a) and second cathode (203b) are different, it is acceptable to remove one of the electrodes at the emission projection and use the remainder as an electron emission electrode. If the emission projections are made thin in this manner, the tip curvature radius in the film thickness direction becomes smaller, allowing lower threshold voltages to be achieved.

A field electron emission device manufactured in accordance with the previous explanation was measured in a high vacuum environment. When the cathode 205 was grounded and the anode cathode voltage was maintained at Vak=200 V with a gate cathode voltage of Vgk=60 V, the cathode current was Ik=4×10^{-8} A. When Vgk=100V, 6× 10^{-5} A was obtained. In addition, the parasite capacitance between cathode 203 and gate electrode 205 was at the order of 10 fF.

In this embodiment, the material employed for the electrodes, such as, for cathode 203, was molybdenum and tantalum thin films. However, this invention is not limited to these particular materials. In addition to these materials, other materials that may be employed are metals, such as, tungsten, silicon, chrome, and aluminium and alloys of these metals. Furthermore, relative to flat substrate 1. Substrate materials, such as, quartz and ceramic substrates having good thermal conductance may be employed. As an example, an insulating substrate or an alumina substrate with an insulator on the surface of a conductive substrate, such as, a silicon substrate, may be employed. Moreover, insulating layer 8 and etching mask 81 are not limited to the employment of a silicon dioxide thin film. Thin films, such as, silicon nitride thin films and alumina thin films may also be employed.

In order to reduce the threshold voltage of the electron emissions, it is also acceptable to coat emission projections 4 with materials that have a small work function, such as barium, thorium and cesium. In addition, cathode 203 may be made of such a material.

In order to reduce the noise from electron emissions, it is possible to create an adequate number of emission projections 4 as well as increase the S/N ratio by driving these and creating electron emissions at the same time. Electron emissions do not have to originate at one point, that is, the tip of the emission projections. They can originate from auxiliary projections created on the side of the tip, and this will provide the same effect. In addition, excessive current flow and noise can be prevented by connecting self-bias resistance or non-linear resistance directly to the cathode.

By putting a fluorescent material on the surface of cathode 7 and forming a light emitting display or by forming a material such as a copper thin film that generates X-rays and exciting this with electron beam, it is possible to create a minute x-ray source. Of course, the manufacturing process described above can be used in the same manner in the tetrode field electron emission device shown in FIG. 1.

As described above, the manufacturing process of the field electron device of this invention provides the following improved advantages:

(1)Compared to fabricating the cathode by over-etching of the cathode layer or by over-etching of the etching mask layer formed on the surface of the cathode layer, it is possible to fabricate emission projections having a smaller tip curvature radius. This is because the etching properties of the etching mask formed on the surface of flat substrate 1 are very isotropic and because etching methods that etch at a fast rate, such as wet etching, can be used. Became it is difficult to apply wet etching to materials such as molybdenum, it is also difficult to form emission projections 4 by means of over-etching of such materials.

(2)Lgk is generally determined by the film thickness of the island shaped insulating layer and the gate electrode. The ability to control the film thickness has increasingly become improved and accurate as LSI(Large Scale Integrated circuit) processing technology has progressed, thereby making it possible to achieve a field electron emission device with

excellent uniformity and a low electron emission threshold voltage. In the technology utilized in conjunction with known emission devices, the achievable limit for Lgk was 0.8 microns. However, as a result of the method of this invention, it is possible to fabricate and obtain a limit for Lgk equal to or below 0.1 microns.

(3)Emission projection with a small tip curvature radius and a low threshold voltage were achieved employing over-etching. In the technology utilized in conjunction with known emission devices, the lowest limit of the tip curvature radius is generally 2000 angstroms. With this invention, it is possible to obtain tip curvature radii of 400 angstroms or smaller.

(4)Employing the characteristics of over-etching, convex areas such as mission projections 4 are a smaller, sharper tip curvature radius. Conversely, the concave areas developed are much smoother. With such characteristics, it is possible to take advantage of the convex and concave areas of the cathode to prevent accidental electron emissions and shorting conditions between the electrodes.

(5)It is possible to create a gate electrode which is self-aligned with the cathode of the emission device thereby allowing a reduction in parasitic capacitance between the electrodes and high-speed operation as well. In particular, by creating the first cathode with low resistivity, the method is suitable for high-speed devices having a low resistance and smaller line delays.

(6)FIG. 6(A) is a plan view of a flat tetrode vacuum tube employing the new tetrode field electron emission device described above. FIG. 6(B) is a cross sectional view along the line of FIG 6(A). The flat tetrode vacuum tube has such a structure in which a flat substrate 1, which has the tetrode field electron emission device described above, and opposite side substrate 14 are provided. These two substrates 1 and 14 are positioned substantially parallel to each other with the use of support 17 provided around their periphery to form a sealed vacuum chamber 23 with walls comprising flat substrate 1, opposite substrate 14, and support 17. Opposite substrate 14 is made of a quartz substrate. On the interior surface of substrate 14 facing into vacuum chamber 23 is formed conductive thin film for the purpose of preventing the accumulation of electrostatic charges. In addition, there is sealing port 16, which seals vacuum chamber 23 after it has been evacuated. Sealing port 16 is sealed off by

melting an Cr and Au alloy within the port opening formed of a Cr/Au thin film. Gettering layer 18 formed of an Al and Ba thin film alloy is previously formed on the surface of opposite substrate 14. After vacuum layer 23 has been completed, it is heated with a laser, evaporating it on the walls of vacuum layer to revive the gettering effect.

Support 17 may be a baked mixture of low melting point glass powder and glass fibers having a diameter of 100 microns. It seals and adheres well to both substrates 1 and 14 and maintains a uniform gap for vacuum chamber 23 at 100 microns.

The external accessed pins of the tetrode field electron emission device, i.e., cathode pin 19, gate pin 20, control pin 21, and anode pin 22, extend outside of vacuum chamber 23 through flat substrate 1 and side wall support 17 by means of thin metal films. The size of the flat tetrode vacuum tube may be about 7 mm in length, 4mm in height and 2.2mm in thickness. Compared to the thermoelectric emission type vacuum tubes of the prior art, it is very small, with a volume of 1/1000 or lower. The degree of vacuum in vacuum chamber 23 may be 1×10^{-7} torr or lower.

Anode 7 is formed on the surface of flat substrate 1. However, the present invention is not limited to this. For example, the anodes may be formed on the surface of the opposite substrate. In this case, control electrode 6 may be placed within vacuum chamber 23 so that it is positioned between emission projection 4 and anode 7.

FIG.7 through FIG. 9 illustrate the electrical properties of the tetrode field electron emission device described above. FIG. 7 is a schematic diagram of a cathode pounded voltage amplifier employing the tetrode field electron emission device of this invention. The previously described tetrode vacuum tube is represented by symbol 30. This indicates that cathodes 3, gate 5, control electrode 6, and anode 7 has been vacuum sealed within vacuum chamber 23.

The method of driving a voltage amplifier that employs a tetrode field electron emission device is as follows. This is to say, cathode 3 is grounded and a positive bias gate voltage 26 (V_{GK}) applied to gate 5. A positive voltage 27 (V_{AK}) is applied to anode 7 through load resistance 28 (R_L). A superimposed control bias voltage 25 (V_{CK}) and series connected

input signal voltage 24 are applied to control electrode 6. An output signal voltage 29(Vout) is obtained at point connected to anode 7 and load resistance 28, which is proportional to input signal 24.

FIG. 8 is a graph showing the electron emission properties of the aforesaid tetrode field electron emission device. This is the result of measuring the dependence of gate current 32 (I_g) and anode current 31 (I_A) on gate voltage 26 of the tetrode field electron emission device. In this case, input signal voltage 24 and control bias voltage 25 is at zero volts in the electrical connection drawing in FIG. 7. Gate current 32 and anode current 31 increase exponentially relative to gate voltage 26, indicating that the emission current is the Fowler-Nordheim (F-N) tunnel current. Anode current 31 is about two digits smaller than gate current 32. In the driving method of the prior art, which controls anode current 31 with gate voltage 26, the electric power conversion efficiency was poor because $I_G > I_A$. In addition, because the transference characteristics are also exponential, it is difficult to use this method in a linear amplifier. For this reason, it came to be that anode current 31 is controlled by the voltage that is applied to control electrode 6.

FIG. 9 is a graph showing the input and output static characteristics of the aforesaid tetrode field electron emission device. This is the result of measuring the dependence of control current 33(I_C) and anode current 34 on control bias voltage 25 of the tetrode field electron emission device. In this case, the gate voltage 26 is at V_{GK}= 140 V, input signal voltage 24 is at zero volts and anode 27 is at V_{AK}= 400 V for the device shown in FIG. 7. Although anode current 34 changes exponentially (non-linearly) in the range of $V_{CK} < 0$, anode current 34 changes in a linear manner in the range of $V_{CK} > 0$, i.e., in the range of $V_{CK} > 0$, anode current 34 is proportional to the voltage applied to control electrode 6. Therefore, this device can be employed as a linear amplifier. Also, control current 33 is 1% or lower compared to anode current 34, yielding a field effect voltage amplifier with excellent input and output power conversion efficiency.

An anode 34 current control mechanism from the field effect of such a control electrode 6 is similar to the grid electrode of the thermoelectronic emission vacuum tube of the prior art, i.e., it is a mechanism in which anode current 34 is controlled by electric field

in the form of a bias gradient formed between control electrode 6 and cathode 3 by means of bias control of electrode 6. If negative voltage is applied to control electrode 6 and a negative electric field is formed in the vicinity of emission projections 4, an repulsion force is applied relative to emitted electrons traveling toward anode 7 and the number of electrons that reach anode 7 will be limited.

Since the electrons that are generated from the cathode have an initial velocity, they will increase quickly in the direction toward the anode. However, if a control electrode with a negative bias is interposed in an intermediate position, electron velocity can be reduced by the negative bias gradient of the control electrode, and actually some of the electrons return to the cathode. At this state , many of the electrons remain in a region between the cathode and the control electrode forming an electron cloud, i.e., a space charge limited region. Electrons that are able to continue toward the anode are limited to those with energy levels higher than the control electrode bias. It is known that the travel of electrons in such a space charge limited region yields very low amounts of noise current The fluctuation of the space charge is small compared to the emission current fluctuation (noise current) from the cathode. In particular, the fluctuation of electrons with a small amount of energy can be ignored. Only some of the electrons, those with a high level of energy, crate noise in the anode current the triode field electron emission devices of the prior art do not have or contain this space charge control region. Most of the electrons that are emitted from the cathode are able to reach the anode(electron transfer through the radiation restricted region). Therefore, the emission current noise is expressed as the anode current noise.

However, if positive voltage is applied to control electrode 6, the strength of the repulsion force of the emitted electrons will weaken and anode current 34 will increase. Incidentally, positive bias gate electrode 5 performs the same role as the space charge grid electrode of the pentode vacuum tubes of the prior art and 20 prevents the retention of a space charge in the of cathode 3. As will be discussed later, in this invention, a control electrode has been added between anode and control electrode 6 to prevent the effects of the secondary electrons from anode 7

The linear and non-linear regions can be properly utilized by means of proper setting

of control bias voltage 25. Operation along the linear region is suitable for a linear amplification faction, such as, a linear amplifier. Operation along the non-linear region is suitable for switching functions. Also, if gate voltage 26 is made small, control bias voltage 25, which provides the border line of the linear and non-linear areas, shifts to the low voltage side. Therefore, there are features, such as, being able to freely 35 select the voltage setting of control bias voltage 25 by making settings as desired to gate voltage 26. However, shown in FIG.8, in the tetrode field electron mission device described above, the gate current is significantly higher than the anode current, and the parasite 40 current that flows to the gate electrode is ineffective.

FIG. 10 is a graph illustrating the anode static characteristics of the multiple electrode field electron emission device of this embodiment. It is the result of measuring the V_{AK}-I_{AK} static characteristics when the gate voltage is V_{GK}=140V, input signal is 0V, and control bias voltage 25 is V_{GK}=20V, 40V, 60V and 80V in the electrical connection diagram in FIG. 7. As is understood from FIG. 10, in the multiple electrode field emission device of this embodiment, I_{AK} becomes almost constant in the V_{AK}> 150V range. Also, I_{AK} increases in proportion to V_{CK}, which is an anode static characteristic that is similar to the thermo-electronic emission pentode vacuum tube of the prior art This characteristic is suitable for linear amplifier applications because the anode resistance is very large and the input and output provide a proportional relationship.

If the load resistance in FIG. 7 is RL=5 kilomega-ohms, load line 36 in the anode electrostatic graphic Illustration of FIG. 10 is realized. The basic functions have been confirmed to be those of an amplifier by means of such a circuit. In other words, when control bias voltage 25 was V_{CK}=40 V and a 20-volt sine wave (V_{in}=20Sin (ωt)V) was applied as input signal 24, a 50V sine wave (V_{out}= -50Sin (ωt) V) was obtained as output signal 29. The voltage amplification ratio was confirmed as 2.5 times the amplification function. When the frequency,ω, was enlarged and the frequency characteristics were measured as an amplifier, the cut off frequency, ω_c, was 100 MHz or higher.

FIG. 11 shows the relationship of gate electrode I_G, anode current I_A and control current I_c to control voltage 25 (V_{CK}). Control current I_C is negative when V_{CK}<V_{GK}. Ion

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current in the vacuum and leak current on the surface of the substrate are possible causes of negative current. However, because the current is stable, it is probably surface leak current between the gates. Anode current I_A monotonously increases in relation to control voltage V_{CK}. When the control voltage is very large, the anode current increases almost proportionally to the anode current. In other words, a linear region has been found for the transference characteristics. It has been discovered that radiation current is nearly constant relative to V_{CK}, and that this radiation current is determined by the gate current and is not influenced by the bias of other electrodes.

FIG. 12 shows the control voltage V_{AK} with the anode characteristics as the parameters. Anode current I_A increases, with dependence on both anode voltage V_{CK} and control voltage V_{CK}, and conforms to the following equation:

$$I_A = K(V_{CK} + V_{AK})^n$$

where K, a and n are constants. The characteristics are the same as those for the thermo-electronic radiation triode vacuum tube in a space charge limited area. By estimating the amplification factor $\mu(= 1/a)$ and the mutual conductance $gm(=dI_A/dI_{CK})$ from the same diagram, when $V_{AK}=330V$ and when $V_{CK}=150V$, they are 1 and 2.6E-10S, respectively. n value was about 1.3. When $V_{CK} > V_{GK}$, there is a tendency for some of the anode current to flow to the control electrode.

In the characteristics of FIG. 12, the values of gm and μ are very small. Practically, values of 1ms or more and 100 or more are respectively demanded. There are a number of ways of improving both of these values. However, in the particular case of gm, it is effective to increase the radiation current.

In order to further increase the voltage amplification factor, increase the mutual conductance, and increase the frequency characteristics, it is necessary to either increase the number of cathode 3 emission projections or devise a structure for gate electrode 5 that reduces the number of ineffective gate electrodes while increasing the anode current . In this embodiment, there are six emission projections 4. However, if, for example, this was increased 10,000 times and the emission current was increased 10,000 fold, the voltage

amplification factor and the mutual conductance would increase approximately 10,000 fold, allowing the frequency characteristics to improve approximately 100 times. To decrease the amount of ineffective gate current, the probability of emitted electrons impacting with gate electrode 5 would be reduced by structuring gate electrode 5 so that it has a smaller width, or providing its structure to be at an inclined plane with an open angle in the direction of the projection of emission projection 4 .

In this embodiment, the electrical connection method employed was to ground cathode 3. However, it should be understood that this is not the only configuration. For example, the connection method can be the grounding of gate electrode 5. FIG. 13 is a electric connection diagram that utilizes the multiple electrode field electron emission device of this embodiment but has its gate electrode 5 ground and a negative voltage from cathode voltage 37 is applied to cathode 3. This connection method is different from one shown in FIG. 7. This is such an amplifier that is easy to employ because the border line of the linear region and the non-linear region do not fluctuate as a result of the emission current.

As shown in FIG. 14, when the radiation current is large, it is possible to utilize a driving method having self-biasing resistance R_{SB} between the cathode and the anode in order to achieve an emission current with little noise. FIG. 15 shows the anode characteristics in this case. A 2 megohm self-bias resistance R_{SB} has been inserted in series with the cathode for stabilizing the emission current. When V_{AG}=-270V. the emission current is 10 micro-amps. Based on these results, the values obtained were gm=10 nS and μ=1.5.

These characteristics have been summarized in Table I below. Relative to the tetrode devices, A corresponds to FIG. 12 and B corresponds to FIG. 15.

TABLE 1

Device		gm	μ	Transference Characteristics
Desired Characteristics		>1ms	>100	Linear
Tetrode	A	0.2ns	1	Nearly linear

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Device		$V_{AG} = 300$ V, $V_{CK} = 150$ V, $I_E = 1$ μA		
	B	10.0ns	1.5	Nearly linear
		$V_{AG} = 300$ V, $V_{CK} = -50$ V, $I_E = 10$ μA		
Triode Device		2.0ns	>100	Non-linear
		$V_{AG} = 300$ V, $V_{CK} = 120$ V, $I_E = 1$ μA		

FIG. 16 is a schematic diagram of a pentode field electron emission device, which includes, in addition relative to the previous described tetrode field electron emission device, a screen electrode S. FIG. 17 shows the anode characteristic for the pentode. Measurements were made under the conditions wherein the number of cathode projections are 10,000, $V_{KG}=$ 140V, cathode current $I_K=20$mA, $V_{SG}=100$V, and $R_L=1$ kilohm. In FIG. 17, if a load of $R_L=80$ kilohms is applied, as illustrated by the dotted line in FIG. 17, the amplification factor is four fold with an operating point of Vi=-40V. A pentode device is characterized by having an node current not fluctuating because even if the anode current does change, the electric field near the control electrode will not change due to the existence of the screen electrode. In other words, the anode resistance r_a increases according to the relationship:

$$r_a = \Delta V_A / \Delta I_A$$

The next described embodiment comprises a hexode field electron emission device and its manufacturing process is also described. FIGS. 18(A),(B)and(C) are schematic diagrams of a flat hexode field electron , and the cross sectional view taken along the line B-B and line C-C , respectively. The device has a structure includeing control electrode 6 and anode 7 between which are formed screen electrode 50 and suppressor electrode 53. In addition, both control electrode 6 and screen electrode 50 include separately columnar shaped control electrodes 64 and columnar shaped screen electrodes 65, which are respectively formed on top of control electrode 6 and screen electrode 50. These columnar shaped electrodes are formed so that they pierce or cross the flat substrate by cathode 3, and their height is at least as high as, if not higher than, the film thickness of island shaped insulating layer 2.

As an example, columnar shaped control electrodes 64 have a column shape with a

diameter of 3 microns and a height of 5 microns. The electrode pitch is 10 microns and is located about 10 microns away from emission projections 4 and are formed between two emission projections. Columnar shaped screen electrodes 65 have a length of 5 microns, a thickness of 3 microns and a height of 5 microns. Each columnar shaped control electrode 64 has been positioned a distance of 10 microns away from one another. Suppressor electrode 53 may have a width of 5 microns and is located between anode 7 and screen electrode 50. The distance of suppressor electrode 53 from screen electron 50 may be about 20 microns and from anode 7 may be about 50 microns.

Cathode 3 includes eight mission projections that are formed with a 5 microns pitch. The thickness of island shape insulating layer 2 is 5,000 angstroms. Gate electrode is formed so that it self aligns with cathode 3. The distance from emission projections 4 is 3,000 angstroms. The width of the tip region is about 2 microns. The distance from the control electrode is 4 microns.

The electrons emitted from cathode 3 due to the electric field of gate electrode 5 is controlled by the electric field applied by control electrode 6, and this field limits the amount of electrons that are able to reach anode 7. Screen electrode 50 is maintained at a constant bias to prevent fluctuations of the electric field of control electrode 6 due to the electric field of anode 7. Suppressor electrode 53 prevents the secondary electrons generated by anode 7 from returning to toward control electrode 6. FIG. 19 is for the purpose of describing the manufacturing process of the hexode field electron emission device of the embodiment. It is a longitudinal cross sectional view of the device after the main fabrication processes have been completed. The following is a description of the manufacturing process.

First, insulating layer 8 and cathode 9 are sequentially formed on the surface of flat substrate 1. Then, photoresist layer 11 is formed(FIG. 19(A)). Flat substrate 1 may be made of alumina. Because a ceramic substrate, just as alumina substrate, is highly insulating and has a large thermal conductance ratio, it is excellent as a substrate for a field electron emission device for handing a large amount electric power. Alternatively, a semi-insulating GaAs substrate and a diamond substrate may be employed for substrate 1. Insulating layer 8 may be a 5,000 angstrom thick silicon dioxide thin film. Cathode 9 may be 1,000 angstrom

thick tantalum (Ta) thin film. Photoresist layer 11 is used to form cathode 3.

Next, cathode layer 9 is formed by means of over-etching to form first cathode (3a), shown in FIG. 19(B). Dry etching may be employed as the means to achieve over-etching. After over-etching in CF_4/O_2 gas=120/100 and at RF power 700 watts for 25 minutes, cathode 9 is over-etched to 1 microns to form emission projections 4 having a tip curvature radius of 300 angstroms.

Next insulating layer 8 is etched in portions to form island shaped insulating layer 2 and to remove photoresist layer 11, as indicated in FIG. 19(C). The method of forming insulating layer 2 is the same as that described in connection with prior embodiments.

Next, columnar forming layer 56 is formed as indicated in FIG. 19(D). Columnar forming layer 56 may be a photosensitive polyimide resin, e.g., negative type PI-410 manufactured by Ube Kosan, of 5 microns in thickness which is formed by means of coating. Alternatively other types of organic materials may be employed and, further, inorganic materials may be employed for columnar forming layer 56.

Next, columnar forming layer 56 is photo-etched to form control electrodes 64 and screen electrodes 65 as indicated in FIG. 19(E). If columnar forming layer 56 is itself of a photosensitive material, the layer can be processed to form these electrodes by means of photo-etching. If the material employed for layer 56 is organic material or inorganic material, alternatively, an anisotropic etching method, such as, RIE (reactive ion etching), may be employed.

Next, gate electrode layer 133 is formed using directional particulate deposition and is shown in FIG. 19(F). The directional particulate deposition method is sputtering, which is used to gate electrode layer 133. Gate electrode layer 133 is made of tantalum (Ta) with a film thickness of 2,000 angstroms. In order to form gate electrode layer 133 to cover control electrodes 64 and screen electrodes 65 , gate electrode layer 133 is deposited on the side surfaces of these electrodes.

Finally, gate electrode layer 133 is etched to form second cathode (3b), gate electrode 5, control electrode 6, columnar shaped control electrodes 54, screen electrode 50, columnar

shaped screen electrodes 65 and suppressor electrode 53 as shown in FIG. 19(G). If columnar shaped control electrodes 64 and columnar shaped screen electrodes 65 are made of an organic material, a high vacuum condition cannot be maintained until they are removed. The method of their removal is as follows. First, the surface of flat substrate 1 is coated with resist material. At this time, the thickness of the resist formed at the tips of columnar shaped control electrodes 64 and columnar shaped screen electrodes 65 is thinner compared to other areas of these electrode structures. Then, this resist material is removed by means of dry etching and the tips of columnar shaped electrodes and gate electrode layer 133 will first appear. When gate electrode layer 133 is removed by etching, apertures are formed in and through the tips of each electrode. Finally, these electrode columns are removed by use of a solvent. Because the columnar shaped electrodes produced in this manner are hollow and no longer have organic materials a source of outgassing so that a high vacuum condition can be created and maintained by a (heating and vacuumizing) method.

FIG. 20 is a perspective view of a hexode vacuum tube having a hexode field electron emission device structure of this embodiment. In this case, the hexode field electron emission device is vacuum packed into a metal can. This is to say, flat substrate 111 which supports the hexode field electron emission device is fixed in place by a hermetic seal. Wires 162 connect each electrode to a hermetic pin 161. Hermetic seal 160 and cap 163 are sealed in a vacuum to form vacuum chamber 164. In order to continue to maintain a high vacuum condition, gettering material 165 is formed   and [reduced] on the inner wall of cap 163.

FIG. 21 is a electric connection diagram of a cathode grounded type voltage amplifier. FIG.21 shows the hexode vacuum tube of FIG. 18 indicated symbol 66.As shown, cathode 3, gate electrode 5, control electrode 6, screen electrode 50, suppressor electrode 53 and anode 7 are all vacuum sealed within vacuum chamber 164. Cathode 3 and suppressor electrode 53 are both grounded. A positive bias gate voltage 26 is applied to gate electrode 5. A superimposed control bias voltage 25 and input signal voltage 24 are applied to control electrode 6. An anode voltage 27 is applied to anode 7 through load resistance 28. A desired positive bias is be placed on screen electrode 50. However, for the sake of simplicity, in terms

of the number of power supply sources and the numbers of lines, the positive bias can be made the same bias as that for gate electrode 5(V_{GK}). It is possible for the connection of cathode 5 and suppressor electrode 53 and gate electrode 5 and screen electrode 50 to be provided on the surface of flat substrate 1 or inside of vacuum chamber 164. Although this is a hexode type of device, as connected, the number of pins and the number of power supplies are the same as the previously described tetrode vacuum tube.

The method of driving the hexode field electron emission device is as follows. First, if a constant gate voltage 26 is applied to gate electrode 5, a constant or steady state amount of electrons will be emitted or ejected from cathode 3. As long as gate voltage 26 does not change, the volume of ejected electrons remains constant. In this condition, with anode voltage 27 constant, if input signal 24, which has direct current bias, is applied to control electrode 6, the anode current is controlled in proportion to input signal 24 and output signal voltage 29, which is amplified through load resistance 28. The field effect of the electrons of control electrode 6 will be the same as the effect described in connection with previous embodiments. Screen electrode 50 prevents field fluctuations due to voltage fluctuations in the vicinity of control electrode 6. It also has the function of improving the anode resistance and the frequency characteristics. Suppressor electrode 53 prevents the secondary electrons generated by anode 7 from flowing in toward or to control electrode 50.

When the hexode field electron emission device is driven at V_{AK} =300 V, V_{GK} =160 V, V_{KG} =60 V, and R_L =1 kilomega-ohm, a voltage amplification factor of μ=8 is achieved. In this case, the mutual conductance gm=2×10^{-9}S. The frequency characteristics are improved two fold compared to the tetrode field electron emission device described in the previous embodiment. This is believed to be due to the anode screening effect of screen electrode 50.

FIG. 22 shows another schematic diagram of the hexode field electron emission device. FIG. 23 is a graph showing its anode characteristics, which was measured under the conditions of 10,000 cathode emission projections, V_{KG}=-140 V, cathode current, I_K =20 mA, V_{SG} =100 V and R_L =1 kilohm. As is clear from comparison of FIG. 23 and FIG. 17, the anode resistance further increases due to the presence of the suppressor electrode, and saturation properties are indicated even if V_{AG} is small. The anode resistance was 8

megaohm.

This invention does not only apply to the flat devices described above. It can also apply to vertical devices. As one example, a vertical tetrode field electron emission device formed on a silicon single crystal substrate will be described in this embodiment.

FIG. 24 is an illustration of this invention in the form of a vertical tetrode field electron emission device. The device generally comprises a conductive flat substrate 40, for example, of an n-type single crystal silicon substrate with a (100) surface; cathode 41, formed on the surface of flat substrate 40, which has a pointed shape projecting upward in a vertical direction; first insulating layer (42), formed on the surface of flat substrate 40 and surrounding the opening at the circumference of cathode 41; gate electrode 43, formed on the surface of first insulating layer (42) and surrounding the opening at the circumference of cathode 41; second insulating layer (44), formed on the surface of gate electrode 43 and surrounding the opening at the circumference of cathode 41; control electrode 45, formed on the surface of second insulating layer (44) and surrounding the opening at the circumference of cathode 41; and opposite substrate 46, on which is formed anode 47, which is located on the opposed side of the vacuum layer 48 which is at the control electrode 45.

The result of the anisotropic etching of flat substrate 40 is a substantially conical shaped anode 41 whose plumb axis is perpendicular to the surface of flat substrate 40 and has a height of about 1.2 microns. Its cross sectional apex angle is about 90 degrees. In the alternative, cathode 41 may be formed by other methods of fabrication in this invention. For example, the cathode may be Spindle type. First insulating layer (42) and second insulating layer (44) may be made of silicon dioxide thin film having respective thickness of 6,000 angstroms and 3 microns. The diameter of the openings formed in both insulating layers are approximately the same, e.g., 3 microns. Gate electrode 43 and control electrode 45 may be made from molybdenum with respective film thickness of 2,000 angstroms and 3,000 angstroms. The diameter of the opening forming each electrode 43 and 45 may be the same, e.g., about 1.2 microns. Flat substrate 40 and opposite substrate 46 are attached relative to each other by means of a support which surrounding their out circumference. Vacuum chamber 48 is formed between them. The spatial depth of vacuum region 48 is 50 microns.

Anode 47 may be a transparent conductive aluminum film.

The operating functions of the tetrode field electron emission device of FIG. 24 are as follows. Relative to cathode 41, when a positive bias is applied to gate electrode 43, electrons are ejected from the projecting tip of cathode 41. These emitted electrons pass through the openings forming gate electrode 43 and control electrode 45 and arrive at anode 47. However, the amount of electrons, i.e., the anode current, that are able to reach anode 7 can be controlled by the bias voltage placed on control electrode 45. The anode current control due to the field effect of control electrode 45 functionally operates in the same manner as control electrode 6 in the first embodiment. Therefore, a linear region exists wherein the applied voltage of control electrode 45 and the anode current are proportional to each other. In other words, when the voltage of control electrode 45 is sufficiently negative, a negative bias gradient is created out from control electrode 45 in a direction toward cathode 41 and the ejected electrons are bounced back in a direction toward gate electrode 43. In such a situation, therefore, the anode current is small. However, when the voltage of control electrode 45 is sufficiently, a positive bias gradient is created so that any electrons will pass beyond control electrode 45 toward anode 47 creating a large anode current.

The electrical operating characteristics of a tetrode field electron emission device of the embodiment were measured using an emission device having 10,000 cathodes 41. In a circuit configuration where the cathode is grounded, with an applied gate voltage of 120 V, an anode current of 3 mA was obtained. The change in the anode current relative to the voltage applied to control electrode 45, i.e., the mutual conductance, was $gm=20$ μs. The parasitic current that flowed to gate electrode 43 was one percent or less indicating the excellent characteristics that are achieved.

It is also recognized that if a screen electrode and a suppressor electrode are utilized in the tetrode field electron emission device, its electrical operating characteristics can be improved. Also, in the foregoing embodiment, anode 47 is formed on an opposing substrate 46. However, alternatively, anode 47 may be formed on the flat surface of substrate 40. In this case, control electrode 45 may be disposed between anode 47 and gate electrode 43. For example, It may be located on the middle of the vacuum layer 48. Additionally, in order to

reduce capacitance between overlapping electrodes, high frequency characteristic and pressure resistance, it is suitable that interconnection is formed on the base of the film cathode 41 to remove excessive regions and overlapping regions. In this case one insulating flat substrate 40 is used.

As with the tetrode field electron emission device of the embodiment, the multiple electrode field electron emission device is either formed so that gate electrode 43 is perpendicular to the direction of electron emissions from cathode 41 or formed so that the opening of gate electrode 43 surrounds the route of flow of the electrons, reducing the parasite current that flows to gate electrode 43 and yielding excellent power efficiency. The reason for this is that when the emitted electrons pass by gate electrode 43, they only slightly traverse across a distance with the degree of thickness of gate electrode 43. This is, in part, because the emitted electrons have only a small probability of impacting with gate electrode 43 as they pass through the center of the electrode opening. It would be very effective to apply this type of structure to a horizontally structured, multiple electrode field electron emission device.

In order to increase the mutual conductance of a horizontal multiple electrode tube, for example, it is necessary to devise a gate electrode structure in the tetrode field electron emission device shown in FIG. 1 so that the emission surface area of cathode 3 is larger. However, if the emission surface area is increased, there will be an increase in the number of electrons that flow to gate electrode 5. As a result, the problem is that it is difficult to achieve power amplification having high performance.

FIG. 25 is a perspective view of an enlarged multiple electrode electron emission device that has a horizontally arranged, ringed shaped gate electrode 51. The electrode 51 is formed between cathode 3 and anode 7. Cathode 3 has the same basic structure as described and shown in the embodiment of FIG. 1. Openings 52 are formed in a portion of gate electrode 51 and are substantially aligned with the tips of emission projections 4 of cathode 3. This structure reduces the gate and control currents by passing electrons that are emitted from emission projections 4 through openings 52 thereby allowing a reduction in parasite current and an increase in input resistance.

openings 52 need not be limited to the particular shape shown in FIG. 25. The structure need only be such that ejected electrons are substantially enabled to pass from projections 4 through the electrode apertures. Therefore, openings 52 may be of a circular, square, polygon or other such shape. Even if openings 52 are not formed so as to be substantially in aligned correspondence with emission projections 4 such as in the case, for example, wherein every second opening is formed so as to align with emission projections 4, the electron emission device will still be operational.

As previously indicated in connection with FIG. 8, the poor power conversion ratio of $I_G > I_A$ can be improved on by providing an opening in gate electrode 51 so that a field electron emission device with linear input and output electrostatic properties can be offered. In FIG. 25, as with gate electrode 51, the structure of control electrode 61 is also formed to have aligned openings 62 to permit the emission or anode current to pass through them. Alternatively, control electrode 61 may have a flat electrode structure like that shown in the embodiment of FIG. 1.

In the case of a tetrode field electron emission device with the type of gate electrode structure shown in FIG. 25, it is possible for it to have the linear input and output relationship possessed by the structure shown in FIG. 1. It is possible to drastically reduce the gate current (a gate current of 1/10 or less of the anode current) and drastically reduce the gate parasite current.

An alternate form for control electrode 61 is shown in FIG. 26. Electrode 61 comprises a plurality of columnar shaped control electrodes 63 formed in an aligned arrangement relative to the interval spacing between adjacent openings 52. Control electrodes 63 may be a variety of shapes such as cylindrical, square, conical or pyramid shape in cross section.

The number of electrodes to be formed relative to any embodiment of this invention is optional. Quite naturally, it could be a hexode field electron emission device, for example. It is possible to have the structure of gate electrode 20 of the hexode field electron emission device shown in FIGS. 18(A), 18(B), and 18(C) replaced by the gate electrode 51 structure shown in FIG. 25.

This would produce a device with gate electrode 5 in FIG. 18 being replaced by the gate electrode 51 structure shown in FIG. 25. In such a case, the electrons that are emitted from emission projections 4 would be controlled by the electric field of control electrode 6, and the amount of electrons reaching anode 7 would be controlled by the control electrode bias. Further, screen electrode 50 will be maintained at a constant electrical bias, preventing fluctuation in the electric field of control electrode 6, which is caused by the electric field of anode 7. Suppressor 53 prevents the secondary electrons generated by anode 7 from returning in the direction toward control electrode 6.

However, problems occur in terms of manufacturing three dimensional gate electrode. For example, the gap control is difficult to master in thin film manufacturing technology. Further, the distribution of the electric field between the cathode and the gate electrode is not uniform so that there is a limit to the I_a /I_g characteristics. Moreover, the manufacturing process requires four photo mask steps, necessitating the use of a complex manufacturing technology. For these reasons, and based on the objective of providing a three dimensional electrical field distribution between the cathode and the gate electrode, it is desirable to provide for the manufacture of a gate electrode of uniform construction and also allow for accurate self alignment(even if a electrode is offset from a position, another electrode is provided on a corresponding position).

The following disclosure is about multiple electrode field electron emission device and the process of the device. It achieves a stable electrode and greatly improves the Ia/Ig characteristics. This multiple electrode field electron emission device comprises cathodes that are formed on top of the insulating layer that is formed on the surface of the insulated flat substrate, and that has multiple emission projections that overhang frown the insulating layer, including anodes that are formed on the surface of the flat substrate and which collect the emitted electrons, and comprises a number of columnar shaped gate electrodes that are formed in between the cathodes and the anodes. The emission projections are located between the adjacent gate electrodes and the shape of the gate electrodes corresponds to emission projections on the cathode. The multiple electrode field electron emission device is fabricated by forming an insulating layer and an electrode layer in sequence on the surface

of an insulated flat substrate by leaving a flat pattern of the gate electrodes and applying photoresist. Then, the emission projections are formed by etching beyond the flat pattern using an etching solution that flows from the flat pattern. Lastly, the columnar shaped gate electrodes are formed in a position on the flat pattern and the resist is removed.

FIG. 27(a) is a plan view of another embodiment of the new multiple electrode field electron emission device. FIG. 27(b) is a cross sectional view taken along line a-a of FIG. 27(A). FIG. 27(c) is a cross sectional view taken along line b-b of FIG. 27(a). FIG. 27(d) is a perspective view of an enlarged portion of the device shown in FIG. 27(a). In FIG. 27(a), cathode 303, gate electrode 305, and anode 307 are formed on the flat surface of substrate 1 which comprises quartz. Cathode 303 is formed as a thin film, for example, having a thickness of 2,000 angstroms, on the surface of silicon dioxide island shaped insulating layer 302. Overhanging emission projections 4 are formed in cathode 303. Cathode 303 may be fabricated from two or more thin film layers. For example, cathode 303 may be a molybdenum thin film formed on top of a tungsten thin film. Emission projections 4 have tips that project in the direction of gate electrodes 305 with surfaces substantially parallel with the surface of flat substrate 1. Island shaped insulating layer 302 does not exist below the tip area of emission projections 4. The tip curvature radius of emission projections 4, as viewed from their planar extent, is 400 angstroms or less.

The structure of gate electrodes 305 is formed so as to self aligns with the structure of cathode 303. Relative to the pentagonal column shape of electrodes 305, one corner facing in the direction of cathode 303 has, for example, an angle .θ. in the range from 60 to 90 degrees. Emission projections 4 are formed in the interval between adjacent gate electrodes 305. Therefore, the electrical field distribution in the vicinity of emission projections 4 is laterally symmetrical. If the height, G, of the pentagonal column of gate electrodes 305 is formed so as to be taller than that of cathode 303, the distribution of the electrical field in the area of emission projections 4 will be laterally symmetrical as well as uniform in the vertical direction. As a result, the electrons emitted from emission projections 4 by means of an established electrical field between cathode 303 and gate electrodes 305 will pass through the spatial interval between gate electrodes 305 and arrive in an efficient manner at anode 307.

This will allow a marked reduction in the parasitic current in the gate current, i.e., the I_a / I_g characteristics (power conversion ratio) will be a significantly improved.

The structure of gate electrode 305 is not limited to a pentagonal column shape. The structure can be a column shape wherein a symmetrical electric field is formed in the vicinity of the emission projections 4 and in which the emitted electrons are efficiently emitted to anode 307. Other examples are a triangular column shape or a column shape with a curved back.

In the foregoing embodiment, a flat triode field electron emission device has been disclosed. However, this embodiment can also be easily modified to have a tetrode or pentode type electrode field electron emission structure.

In FIG. 27, gate electrodes 305 are connected by means of gate electrode interconnect 71. As an example of the dimensions for this embodiment, the distance A, between gate electrodes 305, may be about 3 microns. Distance B of the pentagonal column of gate electrodes 305 may be about 5 microns. Distance C may be about 7 microns. Gap D between gate electrode 305 and cathode 3 may be about 1.5 microns. The thickness of the island shaped insulating layer 302 may be about 0.5 microns. The thickness F of electrode 303 may be about 0.1 microns.

Next to be described is the manufacturing process generally. FIGS. 28, 29, and 30 each describes manufacturing steps followed for this embodiment. First, as indicated in FIG. 28(a), a thermal CVD method is used to form silicon dioxide thin film 311 on the surface of substrate1, which is made of quartz glass, etc. Next, a technique, such as, sputtering is employed to form tungsten layer 312 on top of silicon dioxide thin film layer 311. However, the material for this layer is not limited to tungsten. For example, it could be a material, such as, tantalum. After this, as indicated in FIG. 28(b), resist holes 313, remain which have the shape of the cross section of gate electrode columns, and a resist layer 314 is formed. FIG. 28(c) is a cross sectional view taken along the line b-b of FIG. 28(b), in which reference numbers are same as those of FIG 28(a) and (b). When CF_4 gas, etc. is used to etch, tungsten layer 314, which is exposed in resist holes 313 is etched. As a result, as shown in FIG. 29(a), silicon dioxide layer 316 in FIG. 28(c) is exposed.

After this, using an HF type etching solution, silicon dioxide film 316 in FIG. 29(a) is etched. When that film is over-etched, the reverse taper shown by the cross section of silicon dioxide film 311 in FIG. 29(b) is obtained. Next, when tungsten film 312 is etched with a CH$_4$ type etching solution, the etching of the tungsten progresses to dotted lines 317 and 318 shown in FIG. 29(c)which is taken along the line c-c of FIG. 29(d). This results in the formation of cathode emission projections 319. Since the etch solution that flows from resist holes 313 over-etches the tungsten film along the shape of resist holes 313 from both sides of resist holes 313, the tips of emission projections 319, which is part of the cathode that is formed, are sharp. In addition, and the tip position is equally distant from the adjacent resist holes 313. As a result, in the manufacturing process, it possible for the emission projection 319 that is formed to always be positioned in the middle of the adjacent resist hole 313, even though there may be an error in the positioning of resist hole 313. Also, the distribution of the electrical field formed by emission projection 319 and the gate electrode is always laterally symmetrical. That is, it is possible to form the cathode and the gate electrode so that they self align.

After this, a film of molybdenum, etc., the material that forms the gate electrode, is formed using vapor deposition or sputtering to yield molybdenum films 321 and 322. These are shown in the cross section in FIG. 30(a). As for molybdenum film 321, the flat shape is the same as that of the gate electrode, which has the same shape as resist hole 313. Depending on the manufacturing conditions of the vapor deposition or the sputtering, it is possible to form molybdenum film 321 at a height that is higher than tungsten film 312. When resist layer 314 is lifted off, the results are as shown in FIG. 30(a) and FIG. 30(b). The cathode and gate electrodes will be formed as shown in FIG. 27(c).

As for the formation of the anode in this invention, when the area of broken line 317 is etched, and this area is formed through over-etching in the step shown in FIG. 29(c), tungsten film 320 may be used as the anode. In addition, the anode may be fabricated separately. However, in such a case, tungsten film 320 may also be used as the control electrode of a multiple electrode field electron emission device, or it may be eliminated if it is not necessary.

The gate electrode interconnect 71 is fabricated in advance using a photo mask. Therefore, with this manufacturing process, it is possible to fabricate using two photo mask steps, a photo mask step that patterns the gate electrode interconnects and a photo mask step that forms the resist film shown in FIG. 28(b).

The position of the gate electrode interconnection can be placed where desired. Therefore, if it is formed close to the cathode, the electric field between the cathode and the electrode will increase, offering a device with an excellent electric field.

In the step of FIG. 30(a) in the manufacturing process described above, when the molybdenum layer is formed either by vapor deposition or sputtering, sometimes a molybdenum bridge is formed between molybdenum film 321 and molybdenum film 322, as shown in FIG. 31. Since this is not good for the formation of the gate electrode, the manufacturing process should be one that does not form bridge 323.

Such a manufacturing process is shown as an example below. FIG. 32(a) is an enlargement of a section of FIG. 28(C), showing the same manufacturing steps. When the gate electrodes are formed in advance on substrate 1, interconnect pattern 325, which corresponds to the shape of the resist holes, can be fabricated.(The material for interconnect pattern 325 may be, for example, aluminum, but may also be other types of material.)

In this configuration, when silicon dioxide layer 311 is over-etched, as shown in FIG. 32(b), the interconnect pattern is exposed. Therefore, as shown in FIG. 32(c), a thin layer of aluminum 326 is formed on top of the interconnect pattern 325 by means of vapor deposition or sputtering. Aluminum layer 327 is formed on top of resist layer 314.

Next, after tungsten layer 312 is over-etched, as shown in FIG. 32(d), resist layer 314, which is around the periphery of resist hole 328, is removed using oxygen plasma forming the structure as shown in FIG. 32(e). Next, gate electrode metal 329, which is the material for the gate electrode (which may be aluminum or molybdenum) is formed by means of vapor deposition or sputtering as illustrated in FIG. 32(f). After that, the resist may be removed as illustrated in FIG. 32(g). When forming the gate electrode by means of this manufacturing process, the bridge described above is difficult to form because the periphery

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of resist layer 14 is removed.

EFFECT OF THE PRESENT INVENTION

The invention as disclosed in the several embodiments of this invention has the following remarkable advantages.

(1) Because the voltage of the control electrode and the current of the anode are in a linear relationship, the input and output transference characteristics are linear. Further, the anode resistance is very large. As a result, it can be used in a linear amplifier, something that has been difficult with the technology of the prior art.

(2) The parasite current that flows to the gate has been decreased markedly. From the perspective of the consumption of current, it is a multiple electrode field electron emission device which has an effective linear amplification effect.

(3) Because the input resistance of the control electrode is very large, it can be used in field effect amplifiers and switching devices.

(4) Compared to the thermo-electronic emission vacuum tubes of the prior art, the current, voltage, and power that can be handled is either the same or better. In addition, it is very small.

(5) Because mutual conductance and the degree of linearity of the transference characteristics can be controlled by the gate voltage, even using the same device, special parameters can easily form different circuits.

(6) There is a great degree of freedom in configuring a device that responds to an application, such as a device with excellent frequency characteristics, a device with excellent power efficiency, or a device that is able to handle large and small power supplies.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 illustrates a perspective view of a tetrode field electron emission device.

FIG. 2 is a schematic diagram of the steps of manufacture process of the tetrode field electron emission device of FIG. 1.

FIG. 3 is an enlarged perspective view of a portion of a new triode field electron emission device of embodiment of the invention.

FIG. 4 is a schematic diagram of the steps of manufacture process of the tetrode field electron emission device of FIG. 3(longitudinal cross sectional view).

FIG. 5 is a schematic diagram of manufacture steps of FIG. 4.

FIG. 6 illustrates a flat tetrode vacuum tube employing the tetrode field electron emission device of FIG. 1, and a cross section taken along the line A-A.

FIG. 7 is an electrical connection diagram of a cathode grounded device employing a tetrode field electron emission device.

FIG. 8 is a graphic illustration of the electron emission characteristics of the device of FIG. 7.

FIG. 9 is a graphic illustration of the input and output electrostatic characteristics of the device of FIG. 7.

FIG. 10 is a graphic illustration of the anode electrostatic characteristics of the device of FIG. 7.

FIG. 11 is a graphic illustration of the relationship between gate current, anode current, and control current of the control electrode of a tetrode field electron emission device.

FIG. 12 is a graphic illustration of the anode characteristics of the tetrode field electron emission device.

FIG. 13 is an electric connection diagram of another tetrode field electron emission device.

FIG. 14 is an electric connection diagram of still another tetrode field electron emission device.

FIG. 15 is a graphic illustration showing the anode characteristics in the electric connection state of FIG. 14.

FIG. 16 is an electric connection diagram of a pentode field electron emission device.

FIG. 17 is a graphic illustration of the anode characteristics in the electric connection state

of FIG. 16.

FIG. 18(A) is a schematic diagram of a hexode field electron emission device. FIGS. 18(B) and 18(C) are cross sections of the hexode field electron emission device.

FIG. 19 is a schematic diagram illustrating the steps of manufacture for the hexode field electron emission device of FIG. 18.

FIG. 20 is a perspective view of a hexode vacuum tube employing the hexode field electron emission device.

FIG. 21 is an electric connection diagram of the hexode field electron emission device.

FIG. 22 is another electric connection diagram of the hexode field electron emission device.

FIG. 23 is a graphic illustration of the anode characteristics of the device of FIG. 22.

FIG. 24 is a cross sectional view of a vertical tetrode field electron emission device.

FIG. 25 is a perspective view of a tetrode field electron emission device whose gate electrode and control electrode have openings.

FIG. 26 is a perspective view of an embodiment in which the control electrodes illustrated in FIG. 25 have a column shaped electrode structure.

FIG. 27(a) is a plan view of a triode field electron emission device in another embodiment of this invention.

FIG. 27(b) is a cross section of the device of FIG. 27(a) taken along the line a-a of FIG. 27(a).

FIG. 27(c) is a cross section of the device of FIG. 27(a) taken along the line c-c of FIG. 27(a).

FIG. 27(d) is a perspective view of the device.

FIG. 28 is a schematic diagram of the steps of manufacture process of the tetrode field electron emission device of FIG. 27.

FIG. 29 is a schematic diagram of the steps of manufacture process of the tetrode field electron emission device of FIG. 27.

FIG. 30 is a schematic diagram of the steps of manufacture process of the tetrode field

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electron emission device of FIG. 27.

FIG. 31 is a schematic diagram illustrating the formation of a bridge structure in the manufacturing process illustrated in FIG. 29 and FIG. 30.

FIG. 32 is a schematic diagram illustrating how not to form a bridge structure in the manufacturing process illustrated in FIG. 29 and FIG. 30.

FIG. 33 is a schematic diagram of a prior art triode field electron emission device.

NOTE OF THE REFERENCE NUMBERS

1 . flat substrate

2. island shaped insulating layer

3. cathode

3a. first cathode

3b. second cathode

4. emission projection

5. gate electrode

6. control electrode

7. anode

7a. first anode

7b. second anode

What is claimed is:

1. A multiple electrode field electron emission device , characterized by comprising at least: a cathode that ejects electrons by means of field effect ,a gate electrode for applying an electric field on said cathode, an anode for collecting the ejected electrons, and a control electrode disposed between said cathode and said anode for controlling said ejected electrons.

2. The multiple electrode field electron emission device of claim 1, wherein a screen electrode disposed between said control electrode and said anode to electrostatically screen said control electrode and said anode.

3. The multiple electrode filed electron emission device of claim 1, wherein a screen electrode disposed between said control electrode and said anode to electrostatically screen said control electrode and said anode, and a suppressor electrode is disposed between said screen electrode and said anode for controlling secondary electrodes emitted from said anode.

4. A multiple electrode field electron emission device, characterized by comprising at least: an island shaped insulating layer disposed on one surface of an insulated flat substrate; a cathode having an emission projection disposed on a surface of said island shaped insulting layer and overhanging said island shaped insulting layer; a gate electrode disposed on said surface of said flat substrate and being nearly perpendicular to an adjacent region of the emission projection; an anode disposed on said surface of said flat substrate in opposite relation to said cathode, and said gate electrode is located between said anode and said cathode; and a control electrode disposed between said gate electrode and said anode on said surface of said flat substrate.

5. The multiple electrode field electron emission device of claim 4, wherein a screen electrode is disposed between the control electrode and the anode formed on the surface of the flat substrate.

6. The multiple electrode field electron emission device of claim 4, wherein a screen electrode is disposed between the control electrode and the anode formed on the surface of the flat substrate, and a suppressor electrode is disposed between said screen electrode and said anode formed on the surface of the flat substrate.

7 The multiple electrode field electron emission device of claim 4 wherein a portion of said control electrode has a substantially columnar shape on the surface of the flat substrate.

8. The multiple electrode field electron emission device of claim 5 wherein portions of both said control and screen electrodes have a substantially columnar shapes on the surface of the flat substrate.

9. The multiple electrode field electron emission device of claim 6 wherein portions of both said control and screen electrodes have substantially columnar shapes on the surface of the flat substrate.

10. A multiple electrode field electron emission device, characterized by comprising: a plumb shaped cathode disposed on a surface of the conductive flat substrate and having nearly vertical plumb axis; a first insulating layer disposed on the flat substrate and having openings surrounding the peripheral portion of said cathode; a gate electrode layer disposed on the first insulating layer and having openings surrounding the peripheral portion of said cathode; a anode layer disposed on a surface of said opposing substrate formed at a side of a vacuum layer; and a control electrode disposed in between said gate electrode and said anode.

11. A method of driving a multiple electrode field electron emission device characterized by the steps of grounding a cathode; applying a positive bias gate voltage to a gate electrode; applying a positive bias voltage to a anode usually larger than the voltage on the gate; and applying an input signal voltage to the control electrode to control the amount of anode current flow.

12. A method of driving a multiple electrode field electron emission device characterized by the steps of grounding a gate electrode; applying a negative bias gate voltage to a cathode; applying a. positive bias voltage to a anode; and applying an input signal voltage to the control electrode to control the amount of anode current flow.

13. A method of driving a multiple electrode field electron emission device characterized by the steps of grounding a gate electrode; applying a negative bias gate voltage to a cathode through resist connecting with the cathode in series; applying a positive bias voltage to a anode; and applying an input signal voltage to the control electrode to control the amount of anode current flow.

14. A method of driving a multiple electrode field electron emission device characterized by the steps of grounding a gate electrode; applying a negative bias gate voltage to a cathode; applying a positive bias screen voltage to a screen electrode; and applying an input signal voltage to the control electrode to control the amount of anode current flow.

15. A method of driving a multiple electrode field electron emission device characterized by the steps of grounding a cathode and a suppressor electrode; applying a gate voltage to a gate electrode and a screen cathode; applying a anode voltage to a anode; and applying an input signal voltage to the control electrode to control the amount of anode current flow.

16. A multiple electrode field electron emission device comprising a cathode arranged on an insulating layer arranged on a surface of a flat substrate, said cathode having a plurality of emission projections overhanging a portion of said insulating layers; an anode arranged on said flat substrate surface for collecting ejected electrons; a gate electrode arranged between said cathode and said anode and having at least one opening in a region corresponding to an emission projection; and a control electrode arranged between said gate electrode and said anode.

17. A multiple electrode field electron emission device comprising a cathode arranged on an insulating layer arranged on a surface of a flat substrate, said cathode having a plurality of emission projections overhanging a portion of said insulating layers; an anode arranged on said flat substrate surface for collecting ejected electrons; a gate electrode arranged between said cathode and said anode and having at least one opening in a region corresponding to an emission projection; a control electrode arranged between said gate electrode and said anode; and a screen electrode arranged said control electrode and said anode.

18. A multiple electrode field electron emission device comprising a cathode arranged on an insulating layer arranged on a surface of a flat substrate, said cathode having a plurality of emission projections overhanging a portion of said insulating layers; an anode arranged on said flat substrate surface for collecting ejected electrons; a gate electrode arranged between said cathode and said anode and having at least one opening in a region corresponding to an emission projection; a control electrode arranged between said gate electrode and said anode; a screen electrode arranged said control electrode and said anode; and suppresser electrode arranged said screen electrode and said anode.

19. The multiple electrode field electron emission device of claim 16, 17 or 18, wherein the opening is arranged all of the regions corresponding to the plurality of emission projections.

20. The multiple electrode field electron emission device of claim 16, 17 or 18, wherein a second opening is arranged on the control electrode and corresponds to said opening.

21. A method of manufacturing a field electron emission device having a emission projection projecting substantially parallel to a surface of flat substrate, and contains at least an etching mask layer on the surface of flat substrate, a cathode layer arranged the surface of said etching mask layer, said method comprising the steps of: depositing and forming an etching passivation layer on said cathode layer, fabricating the etching mask layer to form an etching mask layer, which has the emission projections, and forming said cathode layers on the flat surface of the etching mask and with emission projections.

22. A method process for a field electron emission device comprising the steps of forming an etching mask layer on the surface of a flat substrate base, forming a cathode layer comprising two layers of mutually different materials on the surface of the etching mask layer, forming a photoresist layer on the surface of said cathode layer, fabricating said cathode layer in the flat shape of said photoresist layer, fabricating said etching mask layer using an over-etching method, fabricating said cathode layer in the shape of the etching mask to form the cathode, removing said etching mask from a lower circumference of the cathode to form said cathode in an eave-shape, a process that forms the gate electrode layer using a particulate deposition method, and a process that fabricates said gate electrode layer to form the gate electrode.

23. A multiple electrode field electron emission device comprising a cathode arranged on an insulating layer arranged on a surface of a fiat substrate, said cathode having a plurality of emission projections having ends overhanging a portion of said insulating layers, an anode arranged on said flat substrate surface for collecting ejected electrons, the multiple electrode field electron emission device has such a structure which has a plurality of columnar shaped gate electrode arranged between said cathode and said anode, wherein said emission projection arranged between adjacent gate electrodes, and said gate electrode is a convex which corresponds to said emission projection on the cathode .

24. The multiple electrode field electron emission device of claim 23, wherein the gate electrode is a pentagonal column shape.

25. The multiple electrode field electron emission device of claim 23, wherein the gate electrode is higher than said emission projection.

26. A manufacturing method for a multiple electrode field electron emission device of claim 23, comprising the steps of: forming an insulating layer and an electrode layer in sequence on the surface of an insulated flat substrate, then, after leaving a flat pattern of the gate electrodes and applying photoresist, emission projections are formed by over-etching the electrode layer and insulating layer, over-etching being realized by using an etching solution so that it penetrates said flat pattern and beyond said flat pattern hence forming the emission projections, next, a columnar shaped gate electrode is formed in a position on the flat pattern and resist is removed.

27. A manufacturing method of claim 26,wherein the resist around the flat pattern is removed before the gate electrode is formed at said position.

Abstract

A multiple electrode field electron emission device is formed on an insulating layer disposed on a surface of an insulated flat substrate and the device includes at least a cathode with multiple of emission projections that overhangs the insulating layer, an anode for collecting electrons ejected from the cathode emission projections formed on the surface of the substrate, a control electrodes formed between the cathode and the anode. The device is fabricated using over-etching and directional particulate deposition techniques.